AST-230

Integrated GPS Baseband Chip

FEATURES

- High performance GPS Baseband
- 8K GPS correlator architecture for enhanced sensitivity and faster time to first fix
- Indoor positioning capability with sensitivity of –163dBm
- Lightning fast positioning with fix times of less than a second
- Accurate time output and in-built disciplining block
- ARM7 based processing engine with upto 90MHz clock speed
- Internal high speed SRAM of 2Mbits and 32Kbits of battery backed SRAM to store configuration parameters
- On-chip industry standard peripherals such as USB 2.0, CAN 2.0, Serial Port, SPI, TWI, UART, GPIO
- Supports low power modes supported by wakeup from system RTC
- Multiple boot mechanisms for desired system configuration
- Scalable system clock frequency to suit processing requirements

PERIPHERALS

- USB 2.0 OTG with FULL SPEED support
- Two UART interfaces, with hardware flow control
- 16 bi-directional GPIOs
- Two Wire Interface (TWI) (I2C compatible)
- SPI
- SPORT
- CAN Controller
- Three Timers
- RTC and Watchdog timers
- ETM7 provides CPU trace and debug support
- JTAG and Multiplexed trace ports – 8 bit trace

APPLICATIONS

AST-230 provides a solid low cost platform for wide variety of applications, which involves GPS and other peripherals. It also provides a timing solution, which can provide highly precise clocks to any system, which require such clocks.

The main segments where AST-230 is an ideal choice is

- Personal Navigation
- Tracking and Fleet management
- Base station timing Solutions
- Automotive applications

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FUNCTIONAL BLOCK DIAGRAM

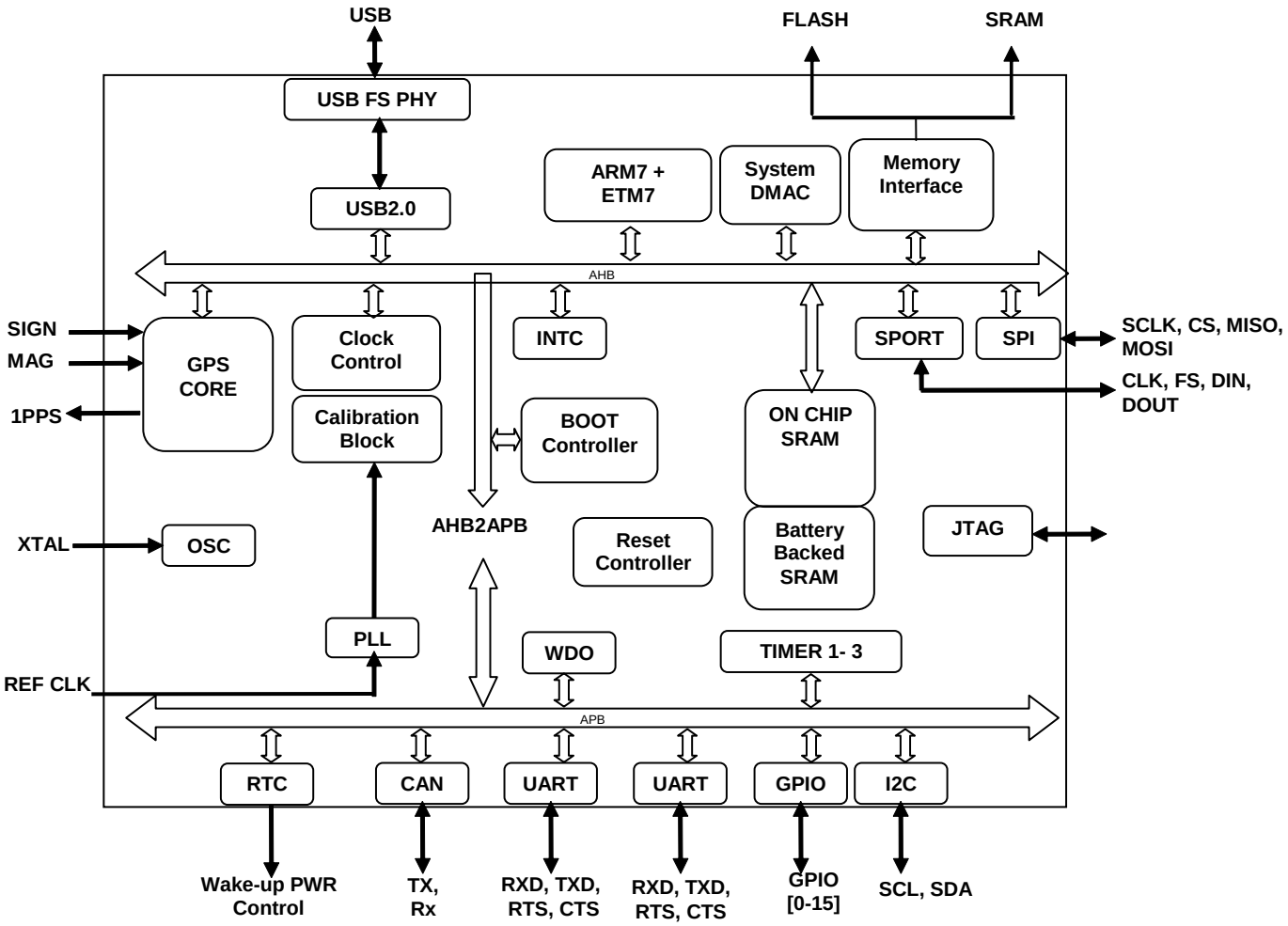

Figure 1: Block Diagram of AST-230

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REVISION HISTORY

June 2017-Revision 1.02

GENERAL DESCRIPTION

AST-230 is a high performance GPS baseband System on Chip aimed at diverse applications in Automotive, Consumer Electronics, Infrastructure, Healthcare and Industrial market segments.

In addition to the GPS baseband, the AST-230 has the highly popular ARM7 processing core along with a host of rich peripherals and on-chip memory to support not just stand-alone functions but also applications combining several functionalities.

The AST-230 also combines several core building blocks such as PLL, Memory Controller, Boot Controller, Reset Controller and 32.768KHz Oscillator to facilitate simpler system integration.

GPS BASEBAND

At the heart of the AST-230 is the GPS baseband. This is a 16-channel correlator capable of interfacing with a standard GPS front-end and processing the GPS signals. The in-built correlators are designed to provide the maximum sensitivity and the shortest time to acquisition, thereby ensuring that the chip delivers unmatched performance. The GPS baseband is seamlessly connected to the ARM7 processing core through the AHB bus to exchange the programming parameters and the correlation results. The GPS firmware running on the ARM7 processing core runs the tracking loops and navigation algorithms using a small memory and MIPS footprint.

In case of transmission errors over the AHB bus, a pin on the AST-230 flags off such occurrences to ensure that incorrect data is not considered by the firmware and also to rectify the situation. In case of an error, the error flag will be held high for 500msec.

CMN_ERROR	Indication
0	No error in communication
1	Error in communication

The GPS core also integrates a 48-bit counter, which runs over the battery power and is clocked by the 32.768KHz oscillator block. The counter is used to maintain precise time to facilitate a fast time to first fix from the GPS core.

The GPS core can be reset by two means –

- Asserting the master reset Mreset_n low for about 2msec
- Asserting the GPS Correlator reset Reset_dsp_b low for about 2msec

In addition, the GPS core provides a built in clock calibration block which is used to calibrate any external clock. This block is highly useful to discipline an external frequency with respect to the precise 1PPS output from the GPS core and derive the long-term accuracy from the GPS system. Disciplining algorithms can run on the ARM7 core and a control loop can be formed to tune the frequency source.

ARM7 PROCESSING CORE

AST-230 contains an ARM7TDMI processing core. The core consists of 16 general-purpose registers of 32-bit width. The ARM7 core is interfaced to several functional blocks such as Interrupt Controller, Memory Controller and DMA Controller to form a complete processing sub-system.

The ARM7TDMI process operates in two modes –

ARM mode: 32-bit word aligned instructions executed in this mode.
Thumb Mode: 16-bit, half-word aligned Thumb instructions executed in this mode.

MEMORY ARCHITECTURE

AST-230 views memory as a single unified 4G-byte address space that can be accessed using 32-bit addressing. All resources, including internal memory, external memory, and I/O control registers occupy separate sections of this common address space.

AST-230 has 2Mbits [256Kbytes] of internal SRAM, of which 32Kbits [4Kbytes] are battery backed up, to store system parameters and GPS data.

The off-chip memory accessed through the Static Memory Controller provides expansion with flash memory and SRAM, optionally accessing up to 16M bits of physical memory.

The System DMA controller provides high-bandwidth data movement capability. It can perform block transfers of code or data between the internal memory and the external memory spaces.

The Peripheral DMA controller provides high-bandwidth data movement capability. It can perform block transfers of code or data between the internal memory and peripheral or vice versa or Peripheral to external memory.

LOW POWER ARCHITECTURE

AST-230 provides power saving options by providing frequency scaling through user control. It employs two power supply domains and ensures that the critical information is retained in the chip through the battery power even when the main power is turned OFF.

SYSTEM INTEGRATION

AST-230 is a highly integrated System on Chip. In addition to the GPS baseband and a host of peripherals,

AST-230 also contains the crucial blocks required for system integration. These are described below.

RTC OSCILLATOR

AST-230 integrates a 32.768KHz oscillator, which is useful to drive an internal Real Time Clock and a battery-backed counter. The oscillator can be driven by a standard crystal of 32.768KHz and is powered from the battery domain.

SYSTEM BUSES

The AST-230 system has two system buses – AHB [ARM AMBA Advanced High Performance Bus], where all the main blocks requiring relatively higher bandwidth are placed and APB [ARM AMBA Advanced Peripheral Bus] where all the low bandwidth peripherals are placed.

CLOCK CONTROL

AST-230 derives all the required internal clocks from an external clock of 16.368MHz. An internal PLL derives a higher system frequency [PLL_CLOCK] of 180.048MHz through which the clocks required by various blocks are derived. The default configuration ensures that the AHB frequency is kept at 90 MHz.

RESET CONTROLLER

AST-230 has an in-built reset controller that generates an active low reset pulse for all internal blocks. The reset controller takes inputs from different sources such as power OFF-ON cycle, watchdog timer expiry and software reset and delivers a single reset pulse. The trigger to the reset controller can be the output of a reset generator external to the AST-230 or a simple RC network.

AST-230 PERIPHERALS

AST-230 contains a rich set of peripherals connected to the core via high bandwidth buses (AHB and APB), providing flexibility in system configuration as well as excellent overall system performance (see Figure 1). The AST-230 processor contains dedicated serial communications ports (SPI, SPORT, TWI and UART) and an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the processor and system to many application scenarios.

USB CORE

AST-230 provides a full speed USB 2.0 OTG controller to support direct connection to a host system at 12M bits per second data rate. The interface provides a flexible programmable environment with up to seven data end points and one control endpoint. Each endpoint can support all of the USB data types and packet sizes including control, bulk, interrupt, and isochronous. The USB OTG feature is supported which allows USB devices to act as a host. When AST-230 is operating as a USB device, it is capable of bus-powered operations. To accomplish this, the USB device must be capable of operations when the core clock and system clock are running at the same frequency as the USB full speed input (60 MHz). This ensures that the AST-230 can run at lowest current until it can request more current from the host. The AST-230 USB controller has dedicated DMA channels and interrupts completion channels to minimize processor polling overhead and to enable asynchronous requests for CPU attention only when transfer management is required.

SPI – SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) is an industry standard synchronous serial link designed to communicate with multiple SPI-compatible devices.

SPI is a 4-wire interface consisting of two data pins, one device select pin, and one clock pin. It is a full duplex, synchronous serial interface, which supports both master and slave modes and can operate in a multi-master environment. This peripheral implementation includes programmable baud rates, clock phase and clock polarity. The SPI is essentially a shift register that serially transmits and receives data bits to/from other SPI devices. During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines.

The SPI block is configured in SLAVE mode by default (after reset). The major applications of SPI in AST-230 are

- Load the boot image by an external host when host boot option is selected
- Load the boot image from an external serial flash when external flash boot option is selected
- As a serial interface for data transfer between SPI-compatible devices

SPORT

AST-230 incorporates one dual-channel synchronous Serial Port (SPORT) for serial and multiprocessor communications.

The SPORT supports the following features:

- Bi-directional operation – Each SPORT has two sets of independent transmit and receive pins, enabling eight channels of I2S stereo audio.
- Buffered (8-deep) transmit and receive ports – Each port has a data register for transferring data words to and from other processor components and shift registers for shifting data in and out of the data registers.
- Clocking – Each transmit and receive port can either use an external serial clock or generate

its own, in frequencies ranging from (fSCLK/131,070) Hz to (fSCLK/2) Hz.

- Word length – Each SPORT supports serial data words from 3 to 32 bits in length, transferred most significant bit first or least significant bit first.
- Framing – Each transmit and receive port can run with or without frame sync signals for each data word. Frame sync signals can be generated internally or externally, active high or low, and with either of two pulse widths and early or late frame sync.
- Interrupts – Each transmit and receive port generates an interrupt upon completing the transfer of a data word or after transferring an entire data buffer, or buffers, through DMA.
- Multi-channel capability – Each SPORT supports 128 channels out of a 1024-channel window and is compatible with the H.100, H.110, MVIP-90, and HMVIP standards.

UARTS

AST-230 integrates two full-duplex universal asynchronous receiver/transmitter (UART) ports, which are fully compatible with PC-standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full duplex, DMA-supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, one or two stop bits, and none, even, or odd parity.

Each UARTport supports following two modes of operation:

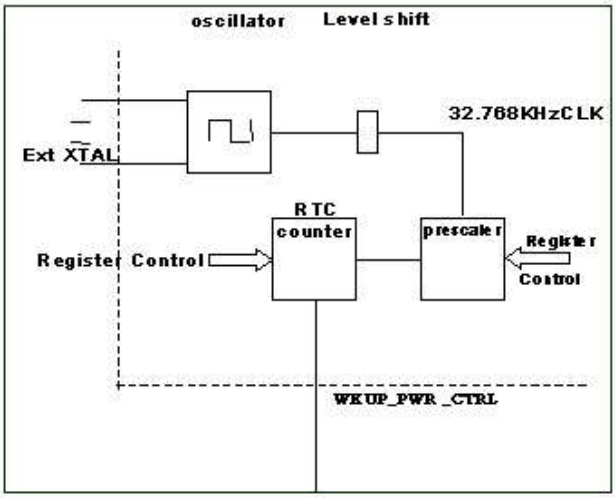
PIO (programmed I/O) – The processor sends or receives data by writing or reading I/O mapped UART registers. The data is double-buffered on both transmit and receive.

DMA (direct memory access) – The DMA controller transfers both transmit and receive data. This reduces the number and frequency of interrupts required to transfer data to and from memory.

Each UART port's baud rate, serial data format, error code generation and status, and interrupts are programmable:

- Supports bit rates ranging from (fSCLK/1,048,576) to (fSCLK/16) bits per second
- Supports data formats from seven to 12 bits per frame
- Both transmit and receive operations can be configured to generate maskable interrupts to the processor

RTC AND WAKEUP TIMER



The Real Time Clock (RTC) provides counters, which gives the real time. The RTC is clocked by a 32.768 kHz crystal external to the AST-230. The RTC Oscillator on-chip generates the required clock frequency output to drive the RTC. The RTC block is powered up by battery backup and clocked even when the rest of the processor is in a low-power state. The RTC contains a 32-bit free running counter, which is clocked by 1Hz signal. It counts up from the initial value of 0x0000000 up to 0xFFFFFFFF and then rolls over to 0x00000000, incrementing by 1 each time a 1Hz tick is seen.

The 32.768 kHz input clock frequency is divided down to a 1Hz signal by a pre-scaler.

The RTC also provides the functionality of a wakeup timer, programming which it is possible to generate events at specified time, which can be used to power down or power up the system.

WATCHDOG TIMER

The watchdog module provides a way of recovery from software crashes. The watchdog clock is used to generate regular interrupt, depending on a programmed value. The watchdog monitors the interrupt and asserts a reset signal if the interrupt remains un-serviced for the entire programmed period. The watchdog can be enabled or disabled as required.

AST-230 includes a 32-bit timer that can be used to implement a software watchdog function. A software watchdog can improve system availability by forcing the processor to a known state through generation of a hardware reset, if the timer expires before being reset by software. The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts to zero from the programmed value. This protects the system from

remaining in an unknown state where software, which would normally reset the timer, has stopped running due to an external noise condition or software error.

The watchdog timer resets both the core and the AST-230 peripherals. After a reset, software can determine if the watchdog was the source of the hardware reset by interrogating a status bit in the watchdog timer control register.

TIMERS

There are three general-purpose programmable timer units in AST-230. These timers can be synchronized to an external clock or to the internal clock. The external timer clock should less than APB clock. The timer units can be used in conjunction with the two UART's to measure the width of the pulses in the data stream to provide a software auto-baud detect function for the respective serial channels. The timers can generate interrupts to the processor core providing periodic events for synchronization.

Any of these three timers can be clocked by the internal processor clock and is typically used as a system tick clock for generation of operating system periodic interrupts.

TWO WIRE INTERFACE

AST-230 includes a two-wire interface (TWI) module for providing a simple exchange method of control data between multiple devices. The TWI is compatible with the widely used I2C™ bus standard. The TWI module offers the capabilities of master and slave operation support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (SCL) and data (SDA) and supports the protocol at speeds up to 400k bits/sec. The default Master/Slave address is 0x00.

The TWI incorporates the following features:

- Simultaneous Master and Slave operation on multiple device systems
- Support of multi master data arbitration
- 7 and 10 bit addressing
- 100 kbits/s and 400 kbits/s data rates
- General Call Address support
- Master Clock synchronization and support for clock low extension
- Separate multiple byte receive and transmit fifo's
- Low interrupt rate
- Individual override control of data and clock lines in the event of bus lock-up
- Single interrupt output request line

GPIO

AST-230 has 16 bi-directional, general-purpose I/O (GPIO) pins allocated across two separate GPIO modules. Each general-purpose port pin can be individually controlled by manipulation of the port control, status, and interrupt registers.

The GPIO module is connected as a peripheral through APB bus. Each GPIO module provides 8-programmable inputs and outputs that can be controlled in two modes.

- Software mode through APB interface
- Hardware mode, through a hardware control interface

The CPU controls the accesses to the data, control and status information of the GPIO through the APB bus interface. When the software control mode is enabled, the data direction register controls the direction of data transfer. When hardware mode is enabled, data direction is controlled through the auxiliary port direction control pins. Similarly, data written and read through this port, but pin status can also be read through the APB interface. The default state of the pins is input.

CAN CONTROLLER

The CAN protocol is an ISO standard (ISO 11898) for serial data communication. The protocol is meant for the automotive applications. CAN protocol has gained widespread use in industrial automation as well.

The interface to the CAN bus is a simple two-wire line. This means, there is an input pin Rx and an output pin Tx. Both pins operate with TTL level and are appropriate for the operation with CAN bus transceivers according to ISO/DIS 11898 or with a modified RS-485 interface.

In the standard implementation, 3 acceptance mask registers and 16 mailboxes are implemented.

The standard features supported by the CAN controller are listed below

- Supports CAN specification 2.0B (active)
- Base data and remote frames
- Extended data and remote frames
- 16 mailboxes for objects of 8-bytes data length
- 4 transmit only mailboxes (mailbox 15 to 12)
- 8 transmit/receive mailboxes (mailbox 11 to 4)
- 4 receive only mailboxes (mailbox 3 to 0)
- One programmable global mask for Message Objects 4 to 11
- Two programmable local masks for Message Objects 0/1 and 2/3
- Acceptance mask register for identifier extension bit
- Receive Message Overwrite Protection
- Priority logic for Transmit Message Objects (Priority defined by mailbox number
- Single Shot Transmission
- Flexible Remote Frame Handling

- Programmable bit rate
- Flexible interrupt structure
- Flexible status interface
- Self Test Mode (Loop back on CAN bus
- Readable error counters. Write access to the CAN error counters (for test purposes)
- 8/16 bit CPU Interface - No wait states (minimum length of CPU signals is required)

BOOTING

AST-230 has three mechanisms for loading the internal memory after reset. The BOOT_MODE pins govern the boot mechanism in AST-230.

- When BOOT_MODE [1:0] = '00': In this case an external host can download the boot image into internal memory via SPI interface. Here the AST-230 acts as SPI slave
- When BOOT_MODE [1:0] = '01': In this case an AST-230 can download the boot image from external SPI flash into internal memory via SPI interface. Here the AST-230 acts as SPI master
- When BOOT_MODE [1:0] = '10': Booting the system from an external parallel flash. Here the start address is re-mapped into the starting location of the external memory; hence the CPU can directly access the image from the external flash.

In all the modes, there is an option for the software to initiate memory BIST before actually downloading the image. The boot loader is supposed to check the status of memory BIST and repair before actually downloading the image.

SPECIFICATIONS

OPERATING CONDITIONS

Parameter	Conditions	Min	Nominal	Max	Units
Internal Supply Voltage		1.08	1.2	1.32	Volts
External Supply Voltage	VIH = 1.7V, VIH_{clock} = 1.9V	2.25	2.5	2.75	Volts
	VIH = 2.2V, VIH_{clock} = 2.4V	2.7	3.0	3.3	
32KHz OSC Supply Voltage		1.08	1.2	1.32	Volts
PLL Supply Voltage		1.08	1.2	1.32	Volts
USB Core Supply		1.08	1.2	1.32	Volts
USB IO Supply		3	3.2	3.3	Volts
High Level Input Voltage (VIH)		1.6		2.8	Volts
Low Level Input Voltage (VIL)		-0.3		+0.7	Volts
Junction Temperature (Tj)		-40	+25	+85	C
High Level output Voltage (VOH) @IOH 4Ma		1.7	1.8		Volts
Low Level output Voltage (VOL) @IOH 4mA			0.2	0.7	Volts
High Level output Current (IOH) @ VOH 1.7 V		7.5	12.3	18.2	mA
High Level output Current (IOH) @ VOL 0.7 V		5.8	9.3	12.9	mA

Table 1: Operating Conditions

ELECTRICAL CHARACERISTICS

Parameter	Test Conditions	Min	Typical	Max	Unit
High Level output Voltage (VOH) @IOH 4mA		1.7			Volts
Low Level output Voltage (VOL) @IOH 4mA		0.7			Volts
High Level output Current (IOH) @ VOH 1.7 V		7.5	12.3	18.2	mA
High Level output Current (IOH) @ VOL 0.7 V		5.8	9.3	12.9	mA
Input capacitance 1) CLK_Ref 2) SCLK 3) SIGN, MAG (GPS) 4) SDIN, RFS, TFS 5) SPORT Output capacitance 1) PTTI (GPS) 2) Other GPS Ports 3) BBC_INT_B 4) SPORT (ARM) 5) SDOUT		 5 10 5 10 10 20 15 15 15 15			 pf

Table 2: Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Rating

Parameter	Rating
Internal Supply Voltage External I/O Supply voltage Input Voltage 1 Input Voltage 2 Output Voltage Swing Load Capacitance Storage temperature range Operating temperature	1.32 V 3.3 V -0.3 to 0.7 V 1.7 to 2.8 V 0 to 3.3 V 20 pf -65 ^{0}C to 150 ^{0}C -40 ^{0}C to 85 ^{0}C

Table 3: Absolute Maximum Rating

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

AST-230 pin definitions are listed in Table 4.

Functional Pin Description

Port Name	Description	Default Value	Pull Up / Pull Down	I/O
CLK_REF	16.368Mhz Clock as PLL Input Clock and Ref Clock for GPS core		NA	I
CLK_IN2	External Clock to Bypass PLL (selected when SEL_CLK_IN2 set to high)		NA	I
CLK_EXT_TIMR	External Clock input for Timers – Not a default clock		NA	I
CLK_EXT_CAL	External clock input from OCXO which needs to be Calibrated		NA	I
CLK_CAL_1HZ	Calibrated 1Hz Clock output	LOW	NA	O
CLK_EXT_CAL_OUT	Calibrated frequency output. CLK_EXT_CAL passing through the same synchronizer logic as CLK_CAL_1HZ to match the on chip delays	LOW	NA	O
CLK_EXT_CAL_DIV	Programmable Clock Outputs (Derivative of CLK_EXT_CAL clock)	LOW	NA	O
CLK_OUT1	Programmable Clock Outputs (Derivative of PLL clock Output)	LOW	NA	O
CLK_OUT2	Programmable Clock Outputs (Derivative of PLL clock Output)	LOW	NA	O
CLK_OUT3	Programmable Clock Outputs (Derivative of PLL clock Output)	LOW	NA	O
CLK_8KHZ	8 KHz Clock Output generated from Reference Clock [CLK_REF]	HIGH	NA	O
RIF_SIF_CLK_OUT	Reserved		NA	
RIF_SYSCLK	Reserved		NA	
CIF_BCLK	Reserved		NA	
SPORT_YCLK	SPORT Y Channel Clock		PD	I/O
SPORT_XCLK	SPORT X Channel Clock		PD	I/O
SPI_CLK	Serial Port Interface Clock		NA	I/O
SEL_CLK_IN2	Signal to Bypass PLL. When Set to 1 selects External Clock [CLK_IN2]		NA	I
MRESET_N	Active Low Asynchronous Master Reset Input		NA	I
RESET_DSP_B	External Asynchronous active low Reset Input for GPS Correlator		PU	I
SPI_FLASH_CS	SPI Flash Chip Select	Z	NA	O
BOOT_MODE_0 BOOT_MODE_1	Boot Mode Selection. 00: booting through SPI host 01: booting through SPI Flash 10: booting through NOR Flash 11: Not Used		NA	I
TEST_MODE [0]			PD	I
TEST_MODE [1]			PD	I
TEST_MODE [2]			PD	I

Table 4: Functional Pin Description

TEST_MODE [3]	PLL_TEST_MODE = 4'b1001 BIST_MODE = 4'b1000 SCAN_MODE0 = 4'b1010 SCAN_MODE1 = 4'b1011 POR_TEST_MODE = 4'b1100 OSC_TEST_MODE = 4'b1101 PHY_TEST_MODE = 4'b1110 BSCAN_MODE_DEF = 4'b1111 For remaining values, the chip is in functional mode		PD	
VDD_ISO_EN	Active Low Signal Indicating VDD is OFF.		PU, PD	I
SMC_CLK_OUT [0]	SMC Clock output for Chip Select 0 Memory [8 or 16-bit Flash Memory only]. Clock not used	LOW	NA	O
SMC_CLK_OUT [1]	SMC Clock output for Chip Select 1 Memory [16-bit SRAM]	LOW	NA	O
SMC_FBCLK	External Memory Feedback Clock [SMC_CLK_OUT [1] to be connected]		PD	I
SMC_DATA [0]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [1]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [2]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [3]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [4]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [5]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [6]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [7]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [8]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [9]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [10]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [11]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [12]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [13]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [14]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_DATA [15]	External Memory Data Bus (For 8-bit flash access on CS0, only lower 8-bits are valid. Access is little-endian)	LOW	NA	I/O
SMC_WAIT	External Memory Active Low Wait Signal		PU	I
SMC_SRAM_MW	External Memory Width Tie-off ['1' indicates 16-bit memory on CS0 and '0' indicates 8-bit memory on CS0]		PU	I
SMC_INT	External Memory Interrupt Pin		PD	I
SMC_WEN	Active Low External Memory Write Enable	HIGH	NA	O

SMC_OEN	Active Low External Memory Output Enable	HIGH	NA	O
SMC_CSN [0]	Chip Select for External Memories (8 or 16-bit Asynchronous Flash memory)	HIGH	NA	O
SMC_CSN [1]	Chip Select For External Memory (16-bit SRAM Memory)	HIGH	NA	O
SMC_ADDR [0]	External Memory Address Bit-0	LOW	NA	O
SMC_ADDR [1]	External Memory Address Bit-1	LOW	NA	O
SMC_ADDR [2]	External Memory Address Bit-2	LOW	NA	O
SMC_ADDR [3]	External Memory Address Bit-3	LOW	NA	O
SMC_ADDR [4]	External Memory Address Bit-4	LOW	NA	O
SMC_ADDR [5]	External Memory Address Bit-5	LOW	NA	O
SMC_ADDR [6]	External Memory Address Bit-6	LOW	NA	O
SMC_ADDR [7]	External Memory Address Bit-7	LOW	NA	O
SMC_ADDR [8]	External Memory Address Bit-8	LOW	NA	O
SMC_ADDR [9]	External Memory Address Bit-9	LOW	NA	O
SMC_ADDR [10]	External Memory Address Bit-10	LOW	NA	O
SMC_ADDR [11]	External Memory Address Bit-11	LOW	NA	O
SMC_ADDR [12]	External Memory Address Bit-12	LOW	NA	O
SMC_ADDR [13]	External Memory Address Bit-13	LOW	NA	O
SMC_ADDR [14]	External Memory Address Bit-14	LOW	NA	O
SMC_ADDR [15]	External Memory Address Bit-15	LOW	NA	O
SMC_ADDR [16]	External Memory Address Bit-16	LOW	NA	O
SMC_ADDR [17]	External Memory Address Bit-17	LOW	NA	O
SMC_ADDR [18]	External Memory Address Bit-18	LOW	NA	O
SMC_ADDR [19]	External Memory Address Bit-19	LOW	NA	O
SMC_ADDR [20]	External Memory Address Bit-20	LOW	NA	O
SMC_BLS_N [0]	Active Low Byte Lane Strobe Signal indicating valid data on bus. When SMC_BLS_N [0] is '0', data on data bus D0-D7 is valid.	HIGH	NA	O
SMC_BLS_N [1]	Active Low Byte Lane Strobe Signal indicating valid data on bus. When SMC_BLS_N [1] is '0', data available on data bus D8-D15 is valid	HIGH	NA	O
SMC_ADV_N	Active Low Address Advance Signal (Used by Few Memories)	HIGH	NA	O
SMC_BAA_N	Active Low Burst Advance Signal for Memories	HIGH	NA	O
SMC_CRE	Configuration Register Enable (CRE), Used by Few Memories	LOW	NA	O
UART1_TXD	UART1 Transmit Output Signal	HIGH	NA	O
UART1_RXD	UART1 Receive input Signal		NA	I
UART1_ RTS	UART1 Request to Send Output Signal	HIGH	NA	O
UART1_CTS	UART1 Clear to Send Input Signal		NA	I
UART2_TXD	UART2 Transmit Output Signal	HIGH	NA	O
UART2_RXD	UART2 Receive input Signal		PU	I
UART2_ RTS	UART2 Request to Send Output Signal	HIGH	NA	O
UART2_CTS	UART2 Clear to Send Input Signal		PU	I
PLL_LOCK_SEL	Signal Indicating whether PLL Lock signal to be considered or not for GPS internal Clocks [when set to 1 - PLL Lock signal used for GPS Internal clocks, 0 - PLL Lock Signal is ignored for GPS clock generation]		NA	I
SIGN	Bit 1 of IF sample from the GPS RF. When using AST-GPSRF, this is driven by the AST-GPSRF on the rising edge of REF_CLK.		NA	I
MAG	Bit 0 of IF sample from the GPS RF. When using AST-GPSRF, this is driven by the AST-GPSRF on the rising edge of REF_CLK		NA	I
PTTI	Precise One second pulse from GPS core	LOW	NA	O
GPS_INT_B	10ms Interrupt to the processor	LOW	NA	O

CMN_ERROR	Communication Flag Status to indicate loss of data integrity between the GPS and ARM cores (If communication checksum fails, indicates to processor with 500msec HIGH output)	LOW	NA	O
BBC_INT_B	Wakeup interrupt from battery backed counter. By default, the BBC_INT_B is high. When programmed from the processor, the interrupt gets generated with falling edge coinciding with required interrupt instant. The width of the pulse will be 1msec	HIGH	NA	O
BOOT_FLSH_ERR_0	Error indication during SPI flash boot option	LOW	NA	O
BOOT_FLSH_ERR_1	Error indication during SPI flash boot option	LOW	NA	O
BOOT_FLSH_ERR_VALID	Valid for Error during SPI flash boot option	LOW	NA	O
GPIO [0]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [1]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [2]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [3]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [4]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [5]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [6]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [7]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [8]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [9]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [10]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [11]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [12]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [13]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [14]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
GPIO [15]	GPIO Pins, which can be configured as either input or output	HIGH	NA	I/O
MOSI	SPI Master Output	Z	NA	I/O
	SPI Slave Input			I/O
MISO	SPI Master Input	X	NA	I/O
	SPI Slave Output			I/O
SPI_CS	SPI Chip Select	Z	NA	I/O
SPORT_XFS	Frame sync for X channel	Z	PD	I/O
SPORT_XADATA	SPORT X channel A data	Z	PD	I/O
SPORT_XBDATA	SPORT X channel B data	Z	PD	I/O
SPORT_YFS	Frame sync for Y channel	Z	PD	I/O
SPORT_YADATA	SPORT Y channel A data	Z	PD	I/O
SPORT_YBDATA	SPORT Y channel B data	Z	PD	I/O
SCL	TWI (I2C compatible) Serial Clock Data	HIGH	NA	I/O
SDA	TWI (I2C compatible) Data Pin	HIGH	NA	I/O
CIF_SDIN	Reserved		NA	
CIF_SDOUT	Reserved		NA	
CIF_FS	Reserved		NA	
RIF_RESET_N	Reserved		NA	
RIF_OSCENOUT	Reserved		NA	

RIF_SIF_EN_OUT	Reserved		NA	
RIF_MOD_SEL[0]	Reserved		NA	
RIF_MOD_SEL[1]	Reserved		NA	
RIF_SIF_DIN	Reserved		NA	
RIF_SIF_DOUT	Reserved		NA	
RIF_RXON	Reserved		NA	
RIF_TXON	Reserved		NA	
RIF_TXRX_DATA	Reserved		NA	
RIF_TXRX_DATA1	Reserved		NA	
RIF_TXRX_DATA2	Reserved		NA	
CANC_TX	CAN Controller TX Data Output	HIGH	NA	O
CANC_RX	CAN Controller Receive Data Input		PD	I
nTRST	JTAG Reset Input		PU	I
TCK	JTAG Clock Input		NA	I
TDI	JTAG Data Input		PU	I
TDO	JTAG Data Output	Z	NA	O
TMS	JTAG MODE Select Input		PU	I
USB_DP	USB D+ line to the PHY		NA	I/O
USB_DM	USB D- line to the PHY		NA	I/O
USB_CID	Device ID detection input pin		NA	I/O
USB_VBUS	VBUS Input pin		NA	I/O
AVDD	Transceiver I/O devices power supply		NA	I
AVSS	Transceiver I/O devices ground		NA	I
VDD	Transceiver core devices power supply		NA	I
VSS	Transceiver core devices ground		NA	I
DRVVBUS	Signals to the external charge pump when in host mode		NA	
CHRGVBUS	Signals to the external charge pump when in host mode		NA	
DISCHRGVBUS	Signals to the external charge pump when in host mode		NA	
XIN	Crystal signal input for RTC, 32.768KHz		NA	I
XOUT	Crystal signal output for RTC, 32.768KHz		NA	O
WKUP_PWR_CTRL	Signal from system RTC (in battery backed up domain). This signal can be used to control the main power control	LOW	NA	O

TIMING SPECIFICATIONS

Tables below describes the timing requirements for the signals used in AST-230 chip. All the peripheral interface timing is also shown below.

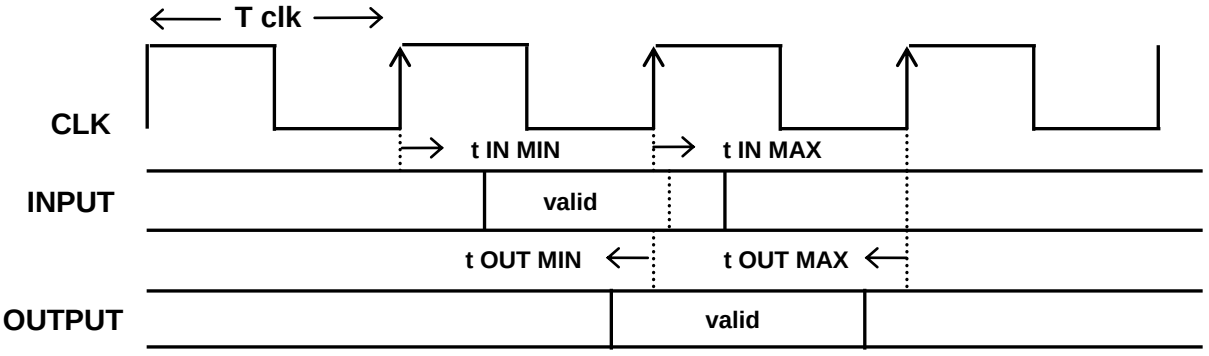


Figure 2: Min and Max Delays with respect to clock

SMC Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
SMC DATA	0	15.56	0	6.78
SMC_WAIT	0	15.56	-	-
SMC_ADDRESS	-	-	0	6.78
SMC_OEN	-	-	0	6.78
SMC_WEN	-	-	0	6.78
SMC_CSN	-	-	0	6.78
SMC_BLS_N	-	-	0	6.78
SMC_ADV_N	-	-	0	6.78
SMC_BAA_N	-	-	0	6.78
tCLK	45MHz			

Table 5: SMC Signals

GPS Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
GPS_SIGN	1	20	-	-
GPS_MAG	1	20	-	-
BBC_INT_B	-	-	0	25
tCLK (clk_ref)	16.368MHz			
tCLK (GPS_SYS_CLK)	72MHz			
tCLK (SCLK)	21MHz			

Table 6: GPS Signals

GPIO Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
GPIO	3	10	1.5	6
tCLK (PCLK)	45Mhz			

Table 7: GPIO Signals

SPI Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max

MOSI	1.6	18.4	1	14
MISO	-1.5	9.5	0	10
SPI_CS	1.5	10	-	-
SPI_FLSH_CS	1.5	10	-	-
tCLK	22.5MHz			

Table 8: SPI Signals

SPORT Signals

Signals (For both Channels)	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
SPORT_XDATA	1	10	0	3
SPORT_XFS	1	10	0	3
SPORT_YDATA	1	10	0	3
SPORT_YFS	1	10	0	3
tCLK	22.5MHz			

Table 9: SPORT Signals

Serial Interface Signals to PCM Codec

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
CIF_SDIN	18	18	-	-
CIF_SDOUT (w.r. to -ve edge of cif_bclk clock)	-	-	13.89	8
CIF_FS (w.r. to -ve edge of cif_bclk clock)	-	-	13.89	8
tCLK	25MHz			

Table 10: Serial Interface Signals to PCM Codec

CAN Controller Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
CANC_TX	-	-	2	6
CANC_RX	3	10	-	-
tCLK (PCLK)	45 MHz			

Table 11: CAN Controller Signals

JTAG Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
TDI	2	12	-	-
TDO	-	-	2	6
TMS	2	12	-	-
tCLK	25 MHz			

Table 12: JTAG Signals

Clock and Reset Timing

Parameter	Minimum Maximum	Unit
Timing Requirements tCKIN CLKIN Period tCKINL CLKIN Low Pulse tCKINH CLKIN High Pulse tWRST RESET Asserted Pulse Width Low	 62 31 31 TBD	ns ns ns ns ns

Table 13: Clock and Reset Timing

Clock and Reset Timing

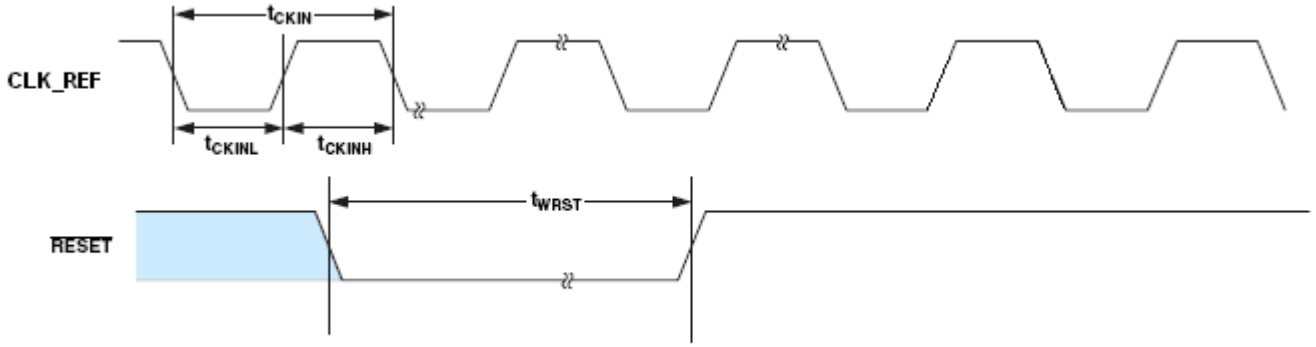


Figure 3: Clock and Reset Timing

Serial Peripheral Interface (SPI) Port—Master Timing

The below table and figure describes SPI port master operations.

Serial Peripheral Interface (SPI) Port—Master Timing

Parameter	V_{DDEXT} = 1.8 V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8 V MBGA Package Min	Max	V_{DDEXT} = 2.5 V/3.3 V All Packages Min	Max	Unit
Timing Requirements							
t_{SSPIDM} Data Input Valid to SCK Edge (Data Input Setup)	10.5		8.5		7.5		ns
t_{HSPIDM} SCK Sampling Edge to Data Input Invalid	–1.5		–1.5		–1.5		ns
Switching Characteristics							
t_{SDSCIM} $\overline{SPISELx}$ Low to First SCK Edge	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICHM} Serial Clock High Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLM} Serial Clock Low Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLK} Serial Clock Period	$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		ns
t_{HDSM} Last SCK Edge to $\overline{SPISELx}$ High	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPITDM} Sequential Transfer Delay	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
$t_{DDSPIDM}$ SCK Edge to Data Out Valid (Data Out Delay)	0	6	0	6	0	6	ns
$t_{HDSPIDM}$ SCK Edge to Data Out Invalid (Data Out Hold)	–1.0	+4.0	–1.0	+4.0	–1.0	+4.0	ns

Table 14: Serial Peripheral Interface (SPI) Port—Master Timing

Serial Peripheral Interface (SPI) Port—Master Timing

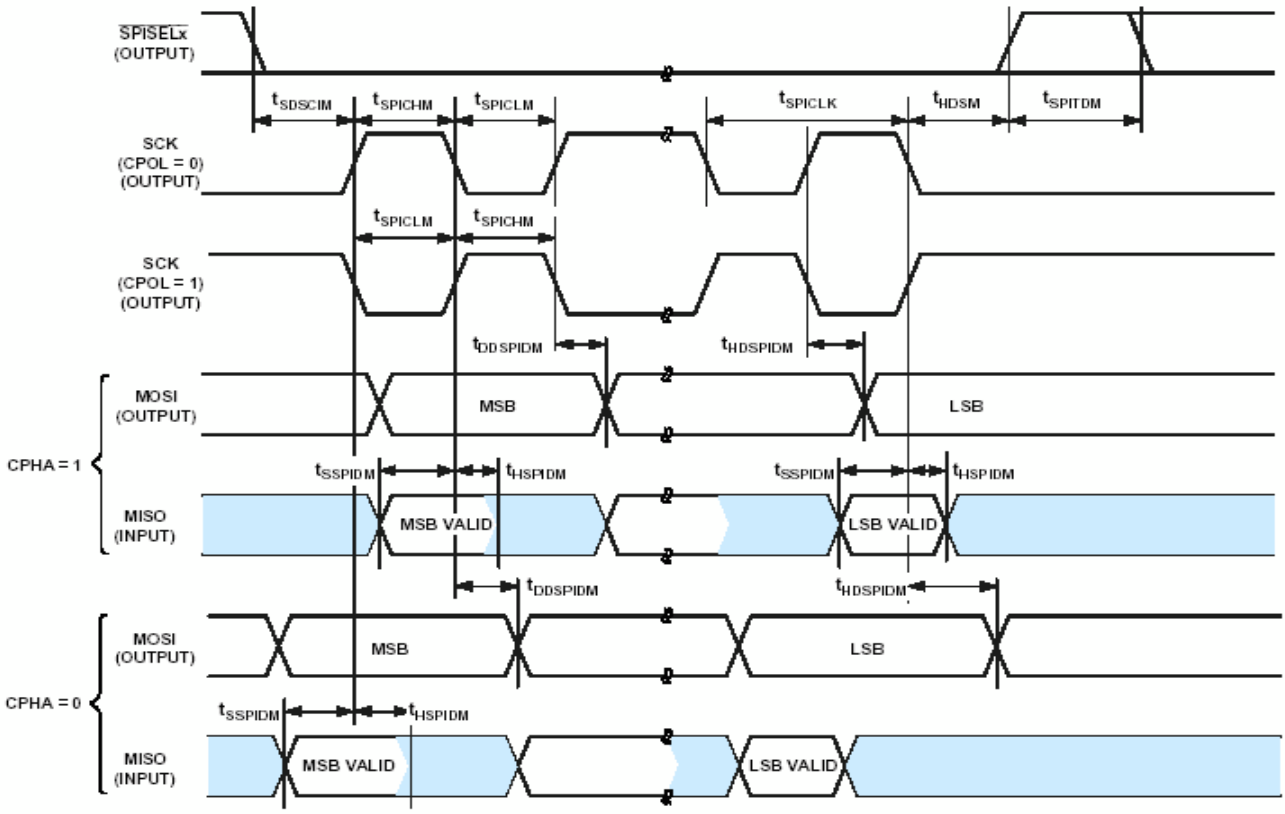


Figure 4: *Serial Peripheral Interface (SPI) Port—Master Timing*

Serial Peripheral Interface (SPI) Port—Slave Timing

Below Table and Figure, describe SPI port slave operations.

Serial Peripheral Interface (SPI) Port—Slave Timing

	V_{DDEXT} = 1.8 V LQFP/PBGA Packages		V_{DDEXT} = 1.8 V MBGA Package		V_{DDEXT} = 2.5 V/3.3 V All Packages		
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Timing Requirements							
t_{SPICHS} Serial Clock High Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLS} Serial Clock Low Period	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPICLK} Serial Clock Period	$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		$4t_{SCLK}-1.5$		ns
t_{HDS} Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SPITDS} Sequential Transfer Delay	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SDSCI} $\overline{SPISS}$ Assertion to First SCK Edge	$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		$2t_{SCLK}-1.5$		ns
t_{SSPID} Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID} SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics							
t_{DSOE} $\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI} $\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID} SCK Edge to Data Out Valid (Data Out Delay)	0	10	0	10	0	10	ns
t_{HDSPID} SCK Edge to Data Out Invalid (Data Out Hold)	0	10	0	10	0	10	ns

Table 15: Serial Peripheral Interface (SPI) Port—Slave Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

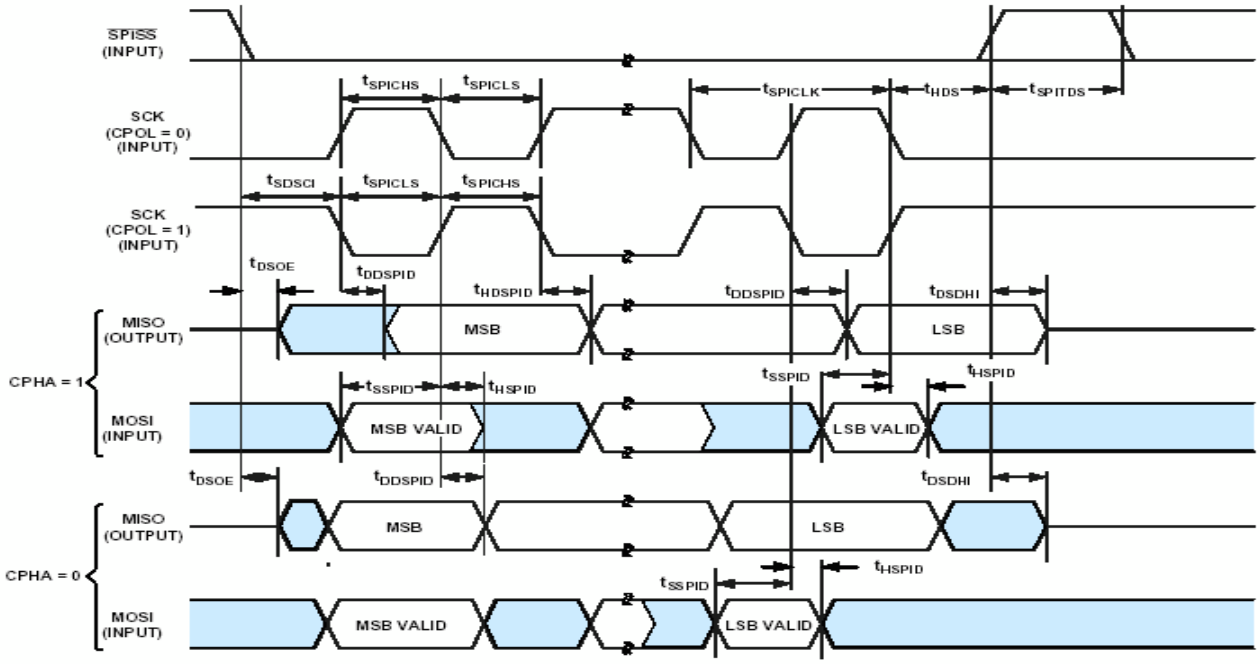


Figure 5: Serial Peripheral Interface (SPI) Port—Slave Timing

JTAG Test and Emulation Port Timing

Below Table and Figure describe JTAG port operations

JTAG Port Timing

Parameter		Minimum	Maximum	Unit
Timing Parameters				
t_{TCK}	TCK Period	40		ns
t_{STAP}	TDI, TMS Setup Before TCK High	28		ns
t_{HTAP}	TDI, TMS Hold After TCK High	2		ns
t_{SSYS}	System Inputs Setup Before TCK High	28		ns
t_{HSYS}	System Inputs Hold After TCK High	2		ns
				TCK
Switching Characteristics				
t_{DTDO}	TDO Delay from TCK Low		18	ns
t_{DSYS}	System Outputs Delay After TCK Low		18	ns

Note: For TDI/TMS Input Delay (Min/Max) and TDO Output Delay (Min/Max) Please refer above.

Table 16: JTAG Port Timing

JTAG Port Timing

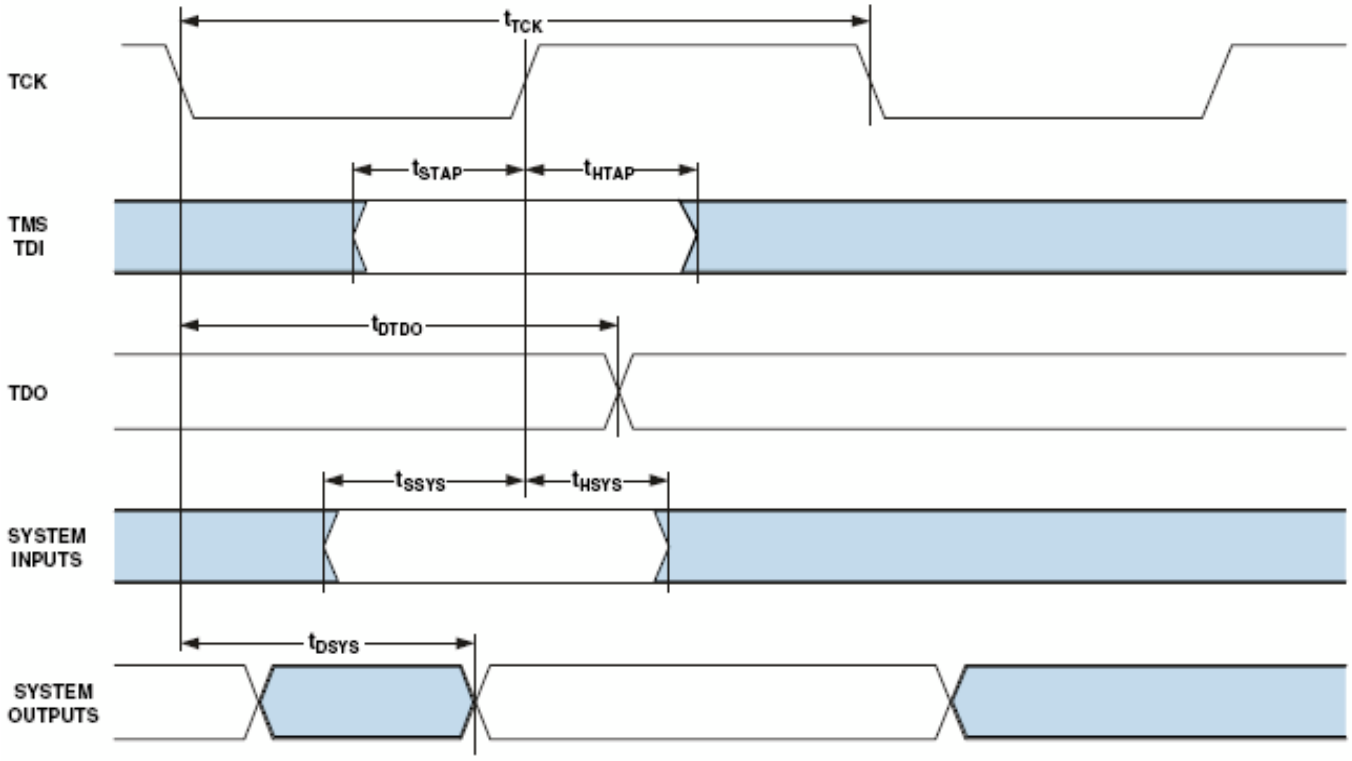


Figure 6: JTAG Port Timing

Memory Controller Timing

The Memory Controller supports various access modes namely

- Asynchronous read
- Asynchronous write
- Synchronous burst read
- Synchronous burst write

The timing Diagram for all the transactions is shown below

Asynchronous Read

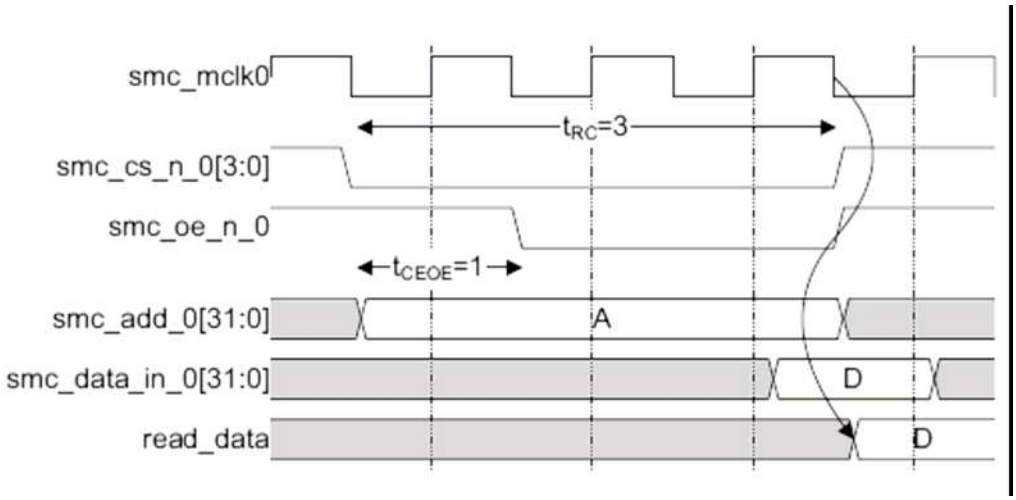


Figure 7: Asynchronous Read

Asynchronous Write

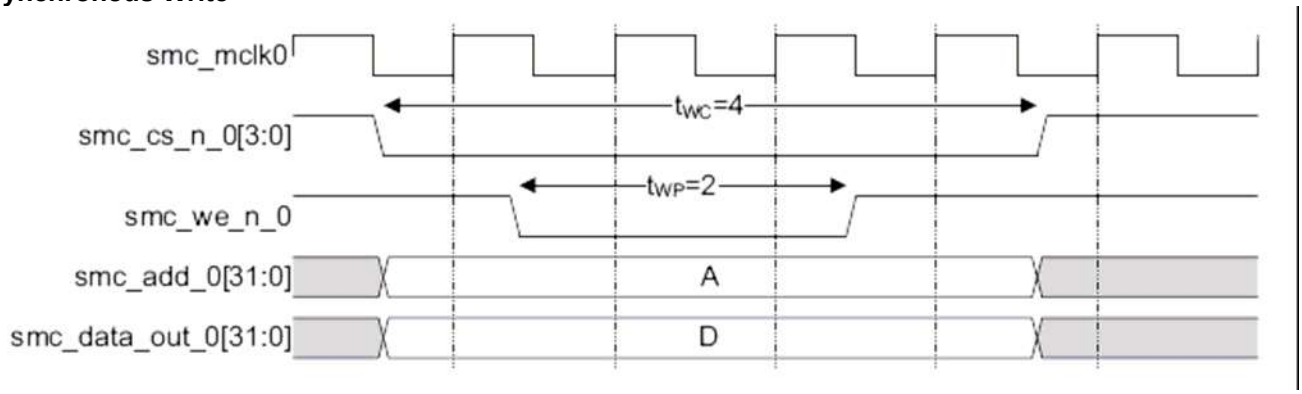


Figure 8: Asynchronous Write

Synchronous Burst Read

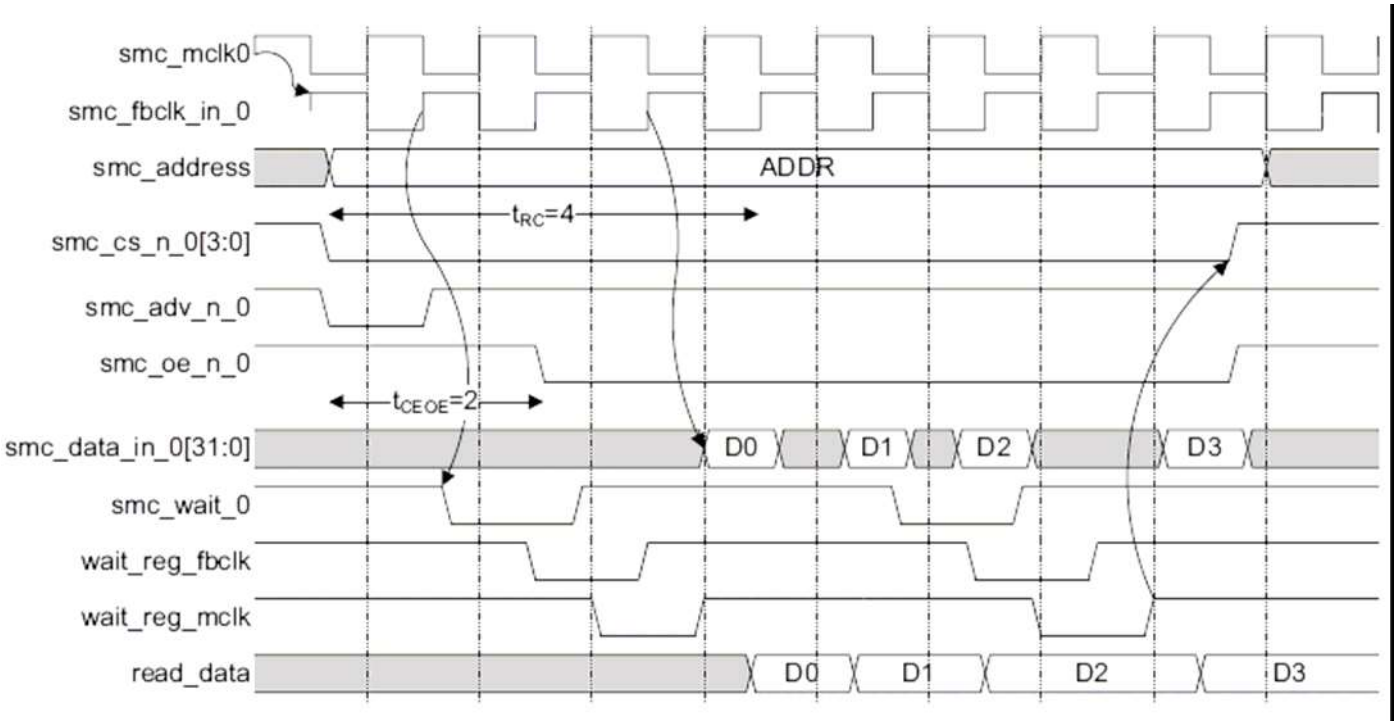


Figure 9: Synchronous Burst Read

Synchronous Burst Write

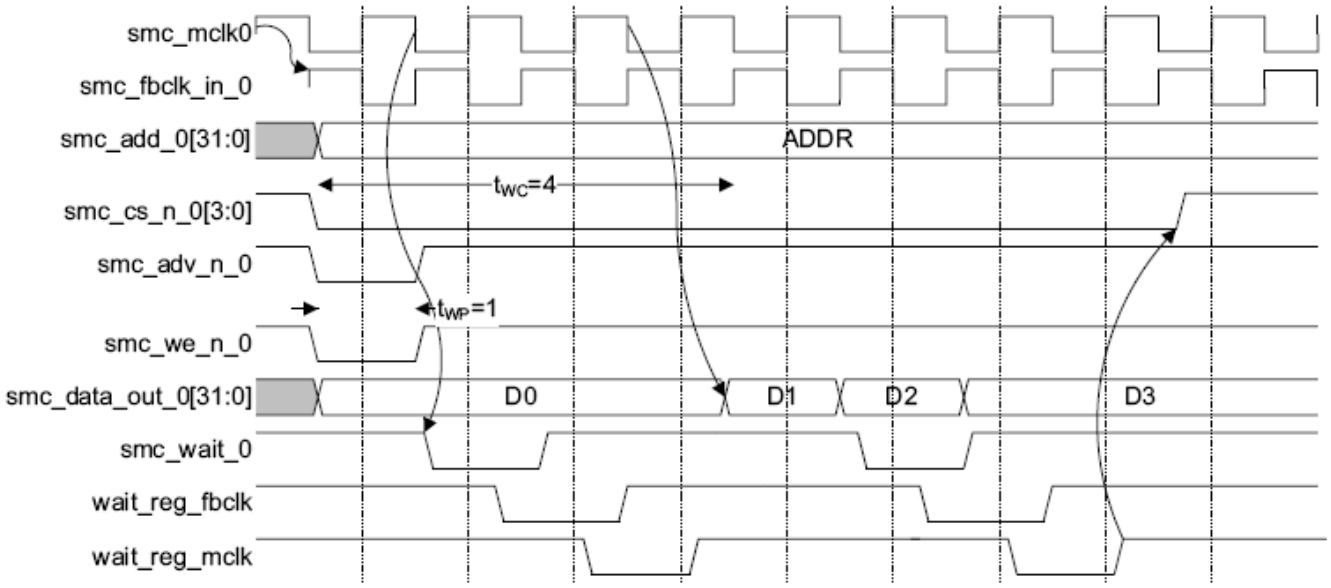


Figure 10: Synchronous Burst Write

196-BALL CSP_BGA BALL ASSIGNMENT

Ball No	Signal Name
A1	GPIO0
A10	CLK_OUT2
A11	GPSINT_B
A12	BOOT_FLSH_ERR_1
A13	BOOT_FLSH_ERR_0
A14	CLK_EXT_CAL_DIV
A2	CIFBCK
A3	RIFTXO
A4	RIFCLK
A5	RIFMOD0
A6	RIFDATA
A7	RIFSIFEN
A8	CLK_EXT_CAL
A9	PTTI
B1	GPIO8
B10	EXT_TIMRCLK
B11	RESET_DSP_B
B12	BOOT_MODE_1
B13	BOOT_FLSH_ERR_VALID
B14	VDD_IO
B2	GPIO6
B3	GPIO1
B4	RIFRSTN
B5	RIFOSC
B6	RIFSIFCK
B7	RIFDATA1
B8	CIFFS
B9	MRESET_N
C1	GPIO14
C10	CLK_OUT3
C11	CMN_ERROR
C12	BOOT_MODE_0
C13	BBC_INT_B
C14	VDD_IO
C2	GPIO9
C3	GPIO7
C4	GPIO4
C5	GPIO2
C6	CIFSD
C7	RIFMOD1
C8	RIFSIFDO
C9	CLK_OUT1
D1	GPIO15
D10	CAL_1HZ
D11	LOCK_SEL
D12	VDD_IO
D13	SMC_ADDR_16
D14	SMC_ADDR_15
D2	GPIO10
D3	GPIO5
D4	GPIO3
D5	GPIO12
D6	RIFRFXO
D7	CIFDIN
D8	CLK_8KHZ
D9	CLK_EXT_CAL_OUT
E1	SIGN
E10	SMC_ADDR_17
E11	SMC_ADDR_18
E12	SMC_ADDR_19
E13	SMC_ADDR_11
E14	SMC_ADDR_10
E2	VSS_IO
E3	VSS_IO
E4	GPIO11
E5	GPIO13
E6	RIFDATA2
E7	RIFSIFDIN
E8	VSS
E9	VSS_IO
F1	MAG
F10	SMC_ADDR_12
F11	SMC_ADDR_13
F12	SMC_ADDR_14
F13	SMC_ADDR_9
F14	SMC_ADDR_8
F2	TEST_MODE3
F3	VSS_IO
F4	TEST_MODE2
F5	VDD_IO
F6	VSS_IO
F7	VSS_IO
F8	VSS
F9	VSS
G1	REF_CLK
G10	SMC_ADDR_5
G11	SMC_ADDR_6
G12	SMC_ADDR_4
G13	SMC_ADDR_3

G14	SMC_ADDR_7
G2	TEST_MODE1
G3	VDD
G4	VDD_POR
G5	CLK_IN2
G6	VSS
G7	VSS
G8	VSS
G9	CANC_RX
H1	SEL_CLK2
H10	SMC_ADDR_20
H11	SMC_ADDR_1
H12	SMC_ADDR_2
H13	SMC_ADDR_0
H14	SMC_WE_N
H2	TEST_MODE0
H3	VSS_POR
H4	VDD_PLL
H5	VSS_PLL
H6	VSS
H7	VDD_IO
H8	VDD_IO
H9	UART2_TXD
J1	TCK
J10	UART1_TXD
J11	UART1_CTS
J12	CANC_TX
J13	SMC_OE_N
J14	SMC_CS_N0
J2	TDO
J3	nTRST
J4	VDD
J5	VDD_VBATT3
J6	VDD_OSC
J7	VDD
J8	UART1_RXD
J9	SDA
K1	TDI
K10	UART2_RXD
K11	UART2_RTS
K12	UART1_RTS
K13	UART2_CTS
K14	SCL
K2	TMS
K3	VSS_VBATT3_IO

K4	WKUP_CTRL
K5	VDD_VBATT
K6	VDD
K7	VDD
K8	SMC_BLS_N1
K9	SMC_INT
L1	XOUT
L10	SMC_ADV_N
L11	SMC_DATA_9
L12	SMC_DATA_7
L13	SMC_DATA_3
L14	SMC_DATA_11
L2	VBATT3_IO
L3	VSS_OSC
L4	VDD_VBATT3
L5	VDD
L6	SMC_BLS_N0
L7	SMC_CRE
L8	SMC_FBCLK_IN
L9	SMC_BAA_N
M1	XIN
M10	VSS
M11	SMC_DATA_2
M12	SMC_DATA_5
M13	SMC_DATA_4
M14	SMC_DATA_10
M2	MISO
M3	SPI_CS
M4	SPORT_YADATA
M5	SPORT_XFS
M6	SPORT_XCLK
M7	USB_DISCHRGVBUS
M8	VBUS
M9	SMC_CLK_OUT1
N1	VDD_ISO_EN
N10	SMC_WAIT
N11	SMC_DATA_1
N12	SMC_DATA_12
N13	SMC_DATA_14
N14	SMC_DATA_15
N2	MOSI
N3	SPI_CLK
N4	SPORT_YBDATA
N5	SPORT_XADATA
N6	USB_DRVVBUS

N7	DM
N8	AVSS
N9	SMC_CLK_OUT0
P1	SPI_FLASH_CS
P10	SMC_SRAM_MW
P11	SMC_DATA_0
P12	SMC_DATA_6
P13	SMC_DATA_8
P14	SMC_DATA_13
P2	SPORT_YCLK
P3	SPORT_YFS
P4	SPORT_XBDATA
P5	SMC_CS_N1
P6	USB_CHRGVBUS
P7	AVDD
P8	DP
P9	CID

Table 17: 196-Ball CSP_BGA Ball Assignment

196-BALL CSP_BGA BALL ASSIGNMENT

Signal Name	Ball No
AVDD	P7
AVSS	N8
CID	P9
DM	N7
DP	P8
BBC_INT_B	C13
BOOT_FLSH_ERR_0	A13
BOOT_FLSH_ERR_1	A12
BOOT_FLSH_ERR_VALID	B13
BOOT_MODE_0	C12
BOOT_MODE_1	B12
CAL_1HZ	D10
CANC_RX	G9
CANC_TX	J12
CIFBCK	A2
CIFDIN	D7
CIFFS	B8
CIFSD	C6
CLK_8KHZ	D8
CLK_EXT_CAL	A8
CLK_EXT_CAL_DIV	A14
CLK_EXT_CAL_OUT	D9
CLK_IN2	G5
CLK_OUT1	C9
SMC_ADDR_0	H13
CLK_OUT2	A10
CLK_OUT3	C10
CMN_ERROR	C11
EXT_TIMRCLK	B10
GPIO0	A1
GPIO1	B3
GPIO10	D2
GPIO11	E4
GPIO12	D5
GPIO13	E5
GPIO14	C1
GPIO15	D1
GPIO2	C5
GPIO3	D4
GPIO4	C4
GPIO5	D3
GPIO6	B2
GPIO7	C3
GPIO8	B1
GPIO9	C2
GPSINT_B	A11
LOCK_SEL	D11
MAG	F1
MISO	M2
MOSI	N2
MRESET_N	B9
nTRST	J3
PTTI	A9
REF_CLK	G1
RESET_DSP_B	B11
RIFCLK	A4
RIFDATA	A6
RIFDATA1	B7
RIFDATA2	E6
RIFMOD0	A5
RIFMOD1	C7
RIFOSC	B5
RIFRFXO	D6
RIFRSTN	B4
RIFSIFCK	B6
RIFSIFDIN	E7
RIFSIFDO	C8
RIFSIFEN	A7
RIFTXO	A3
SCL	K14

SDA	J9
SEL_CLK2	H1
SIGN	E1
SMC_ADDR_1	H11
SMC_ADDR_10	E14
SMC_ADDR_11	E13
SMC_ADDR_12	F10
SMC_ADDR_13	F11
SMC_ADDR_14	F12
SMC_ADDR_15	D14
SMC_ADDR_16	D13
SMC_ADDR_17	E10
SMC_ADDR_18	E11
SMC_ADDR_19	E12
SMC_ADDR_2	H12
SMC_ADDR_20	H10
SMC_ADDR_3	G13
SMC_ADDR_4	G12
SMC_ADDR_5	G10
SMC_ADDR_6	G11
SMC_ADDR_7	G14
SMC_ADDR_8	F14
SMC_ADDR_9	F13
SMC_ADV_N	L10
SMC_BAA_N	L9
SMC_BLS_N0	L6
SMC_BLS_N1	K8
SMC_CLK_OUT0	N9
SMC_CLK_OUT1	M9
SMC_CRE	L7
SMC_CS_N0	J14
SMC_CS_N1	P5
SMC_DATA_0	P11
SMC_DATA_1	N11
SMC_DATA_10	M14
SMC_DATA_11	L14
SMC_DATA_12	N12
SMC_DATA_13	P14
SMC_DATA_14	N13
SMC_DATA_15	N14
SMC_DATA_2	M11
SMC_DATA_3	L13
SMC_DATA_4	M13
SMC_DATA_5	M12
SMC_DATA_6	P12
SMC_DATA_7	L12
SMC_DATA_8	P13
SMC_DATA_9	L11
SMC_FBCLK_IN	L8
SMC_INT	K9
SMC_OE_N	J13
SMC_SRAM_MW	P10
SMC_WAIT	N10
SMC_WE_N	H14
SPI_CLK	N3
SPI_CS	M3
SPI_FLASH_CS	P1
SPORT_XADATA	N5
SPORT_XBDATA	P4
SPORT_XCLK	M6
SPORT_XFS	M5
SPORT_YADATA	M4
SPORT_YBDATA	N4
SPORT_YCLK	P2
SPORT_YFS	P3
TCK	J1
TDI	K1
TDO	J2
TEST_MODE0	H2
TEST_MODE1	G2
TEST_MODE2	F4
TEST_MODE3	F2
TMS	K2
UART1_CTS	J11
UART1_RTS	K12
UART1_RXD	J8
UART1_TXD	J10
UART2_CTS	K13
UART2_RTS	K11
UART2_RXD	K10
UART2_TXD	H9
USB_CHRGVBUS	P6
USB_DISCHRGVBUS	M7
USB_DRVVBUS	N6
VDD_ISO_EN	N1
WKUP_CTRL	K4
VBATT3_IO	L2
VDD	G3
VDD	J4

VDD	J7
VDD	K6
VDD	K7
VDD	L5
VDD_IO	B14
VDD_IO	C14
VDD_IO	D12
VDD_IO	F5
VDD_IO	H7
VDD_IO	H8
VDD_OSC	J6
VDD_PLL	H4
VDD_POR	G4
VDD_VBATT	K5
VDD_VBATT3	J5
VDD_VBATT3	L4
VSS	E8
VSS	F8
VSS	F9
VSS	G6
VSS	G7
VSS	G8
VSS	H6
VSS	M10
VSS_IO	E2
VSS_IO	E3
VSS_IO	E9
VSS_IO	F3
VSS_IO	F6
VSS_IO	F7
VSS_OSC	L3
VSS_PLL	H5
VSS_POR	H3
VSS_VBATT3_IO	K3
VBUS	M8
XIN	M1
XOUT	L1

Table 18: 196-Ball CSP_BGA Ball Assignment

OUTLINE DIMENSIONS

The Package is 12mm X 12mm. Dimensions in below Figure-11 with 196-Ball FBGA are shown in millimeters.

SURFACE MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard

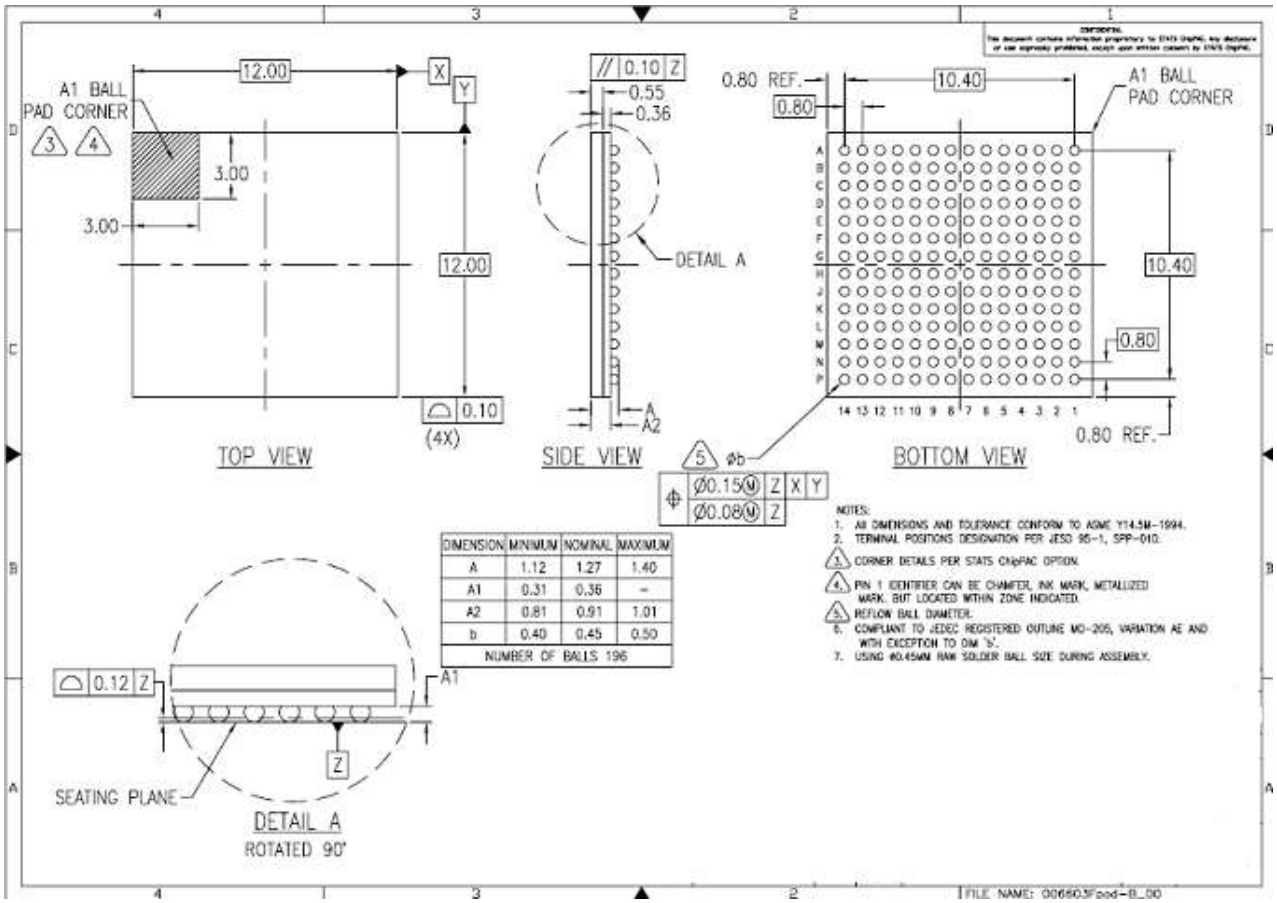


Figure 11: 196 –Ball FBGA

ORDERING GUIDE

Ordering Guide

Model	Temperature Range	Package Description	Package Option	Operating Voltage
AST-230	-40 ^{0}C to +85 ^{0}C	FBGA - 0.8 mm pitch (196 balls), 12.0 mm x 12.0 mm x 1.2 mm	196 balls	1.2 V(Internal), 2.5 V / 3.0 V I/O

Table 19. Ordering Guide