Preliminary Product Brief	**AST-GLSRF** GLONASS RF Downconverter	ACCORD

FEATURES

- Single chip GLONASS downconverter
- GLONASS L1 band (1602 MHz) receiver
- 2.7 V to 3.3 V power supply
- On-chip LNA
- On-chip PLL including complete VCO
- On-chip IF Low Pass Filter
- 50 dB AGC dynamic range
- SIGN and MAGN outputs
- PLL lock information
- Open/Short Antenna control
- Low power operation 15 mA @ 3 Volt
- Internal 26.598MHz sampling clock or optional external sampling clock input

APPLICATIONS

- Automatic vehicle tracking
- Fleet management
- Security applications
- Asset tracking
- Car telematics/navigation
- Marine navigation
- Portable GLONASS receiver

GENERAL DESCRIPTION

The AST-GLSRF is a high performance, fully integrated, RF front-end chip for downconversion and amplification of GLONASS signals. It has been designed for L1 (1602 MHz),

The AST-GLSRF is a superheterodyne receiver, with an on-chip low noise amplifier (LNA), local oscillator, one downconversion IF stage (at 6.120 MHz), an automatic gain controlled amplifier (AGC), an on chip IF low pass filter and a 2-bit analog-to-digital converter (ADC).

The down converter works with 16.368MHz reference clock. The sampling clock for ADC is generated either internally or can be supplied from external source at CKIN.

The down converter has an internal IF low pass filter, which does not require external calibration inputs.

Antenna connection and open circuit can be sensed and the information is made available.

The chip can be interfaced with any active/passive GLONASS antenna.

FUNCTIONAL BLOCK DIAGRAM

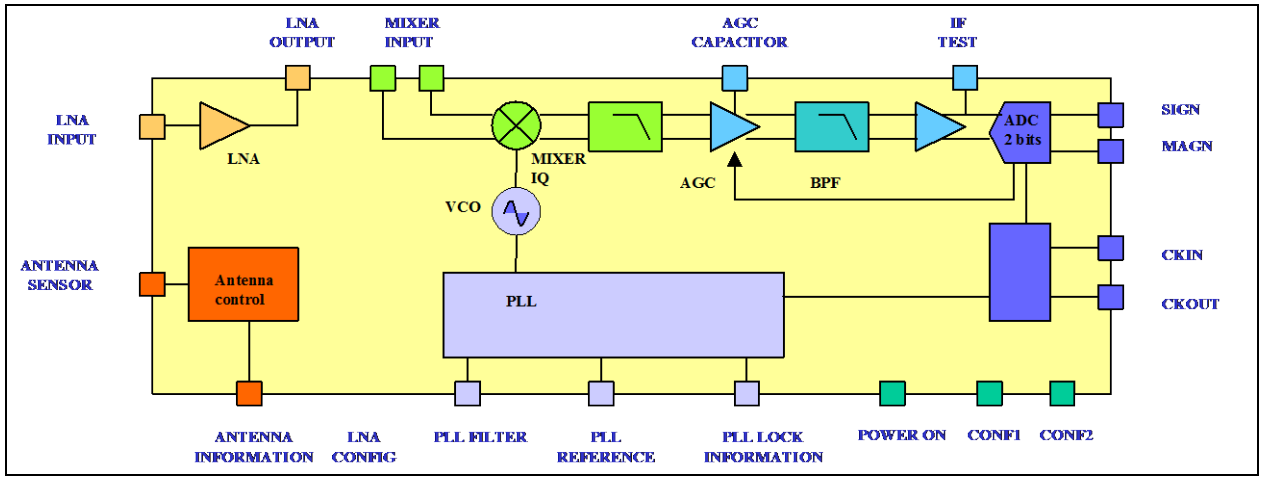

Figure 1. Functional Block Diagram

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

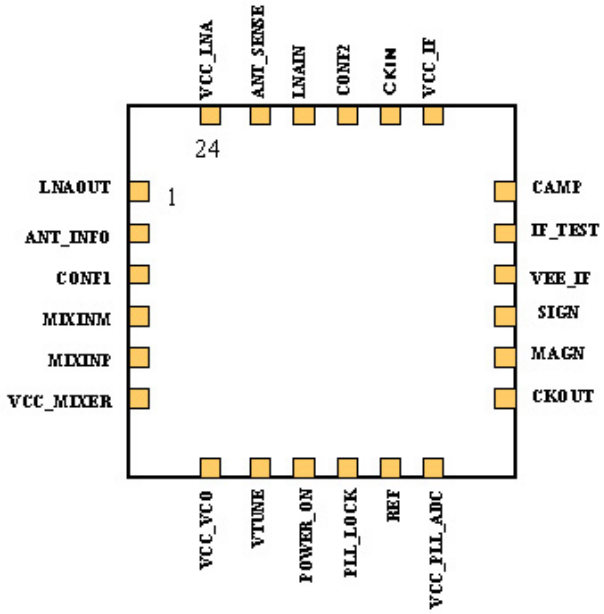

Figure 2. Pin Configuration

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Pin Type	Input / Output	Description
1	LNAOUT	Analog	Output	LNA RF Signal, (1597 – 1606 MHz)
2	ANT_INFO	Analog	Output	Antenna connection information pin
3	CONF1	CMOS	Input	Configuration pin
4	MIXINM	Analog	Input	Positive MIXER RF Signal, (1597 – 1606 MHz)
5	MIXINP	Analog	Input	Negative MIXER RF Signal, (1597 – 1606 MHz)
6	VCC_MIX	Supply		MIXER Supply
7	VCC_VCO	Supply		VCO Supply
8	VTUNE	Analog		External PLL filter connection
9	POWER_ON	CMOS	Input	Power-On mode pin
10	PLL_LOCK	Analog	Output	PLL LOCK information pin
11	REF	Analog	Input	Reference Clock
12	VCC_PLL_ADC	Supply		PLL/ADC Supply
13	CKOUT	CMOS	Output	Reference frequency
14	MAGN	CMOS	Output	Magnitude Bit Data
15	SIGN	CMOS	Output	Sign Bit Data
16	VEE	Ground		Paddle ground internal connection / redundant with exposed pad (paddle)
17	IF_TEST	Analog	Output	IF test
18	CAMP	Analog		Amplitude bit capacitor signal
19	VCC_IF	Supply		IF Supply
20	CLKIN	CMOS	Input	Optional Sampling clock. Selectable with CONF1 and CONF2 combination
21	CONF2	CMOS	Input	Configuration pin
22	LNAIN	Analog	Input	LNA RF Signal, (1597 – 1606 MHz)
23	ANT_SENSE	Analog	Input	Antenna sense for connection control
24	VCC_LNA	Supply		LNA Supply

Table 1. Pin Function Descriptions

PACKAGE INFORMATION

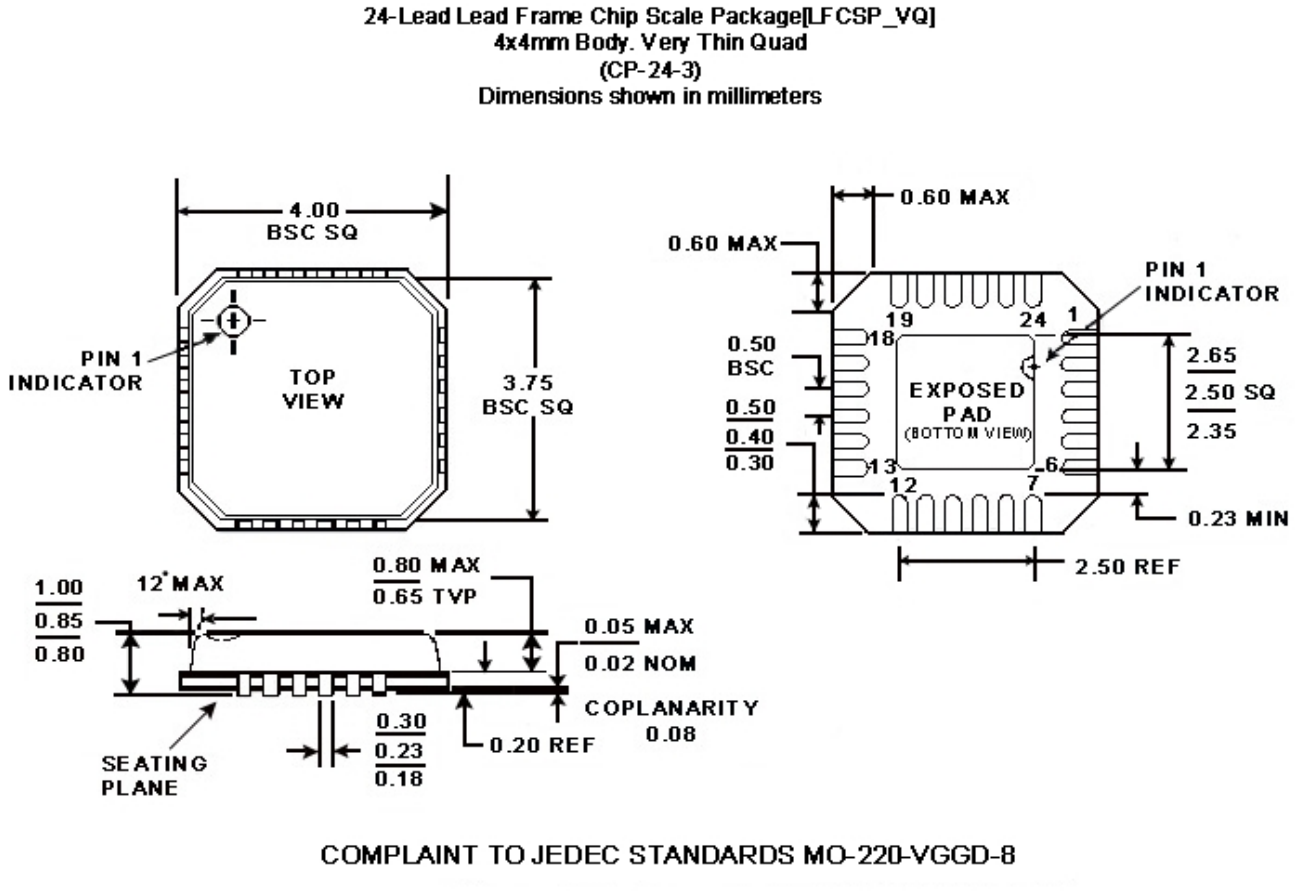

Figure 3. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
AST-GLSRF	3.0 V	−40°C to +85°C	24L LFCSP 4mmx4mmx0.85mm Lead free part	

Table 2. Ordering Guide

APPLICATION SCHEMATIC

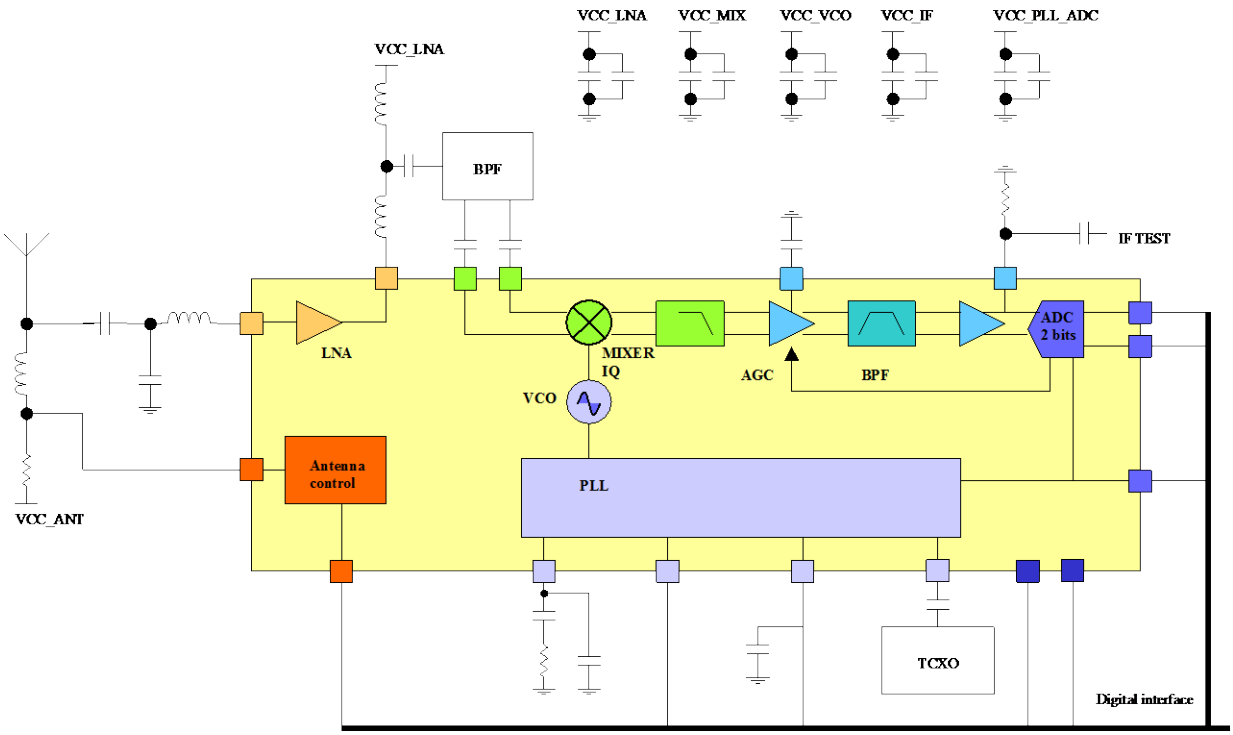

Figure 4. Application schematic