Technical Data

AST-GPSRF

GPS / Galileo RF Downconverter

FEATURES

- Single chip GPS / Galileo downconverter
- GPS L1 band C/A code (1575.42 MHz) receiver
- GALILEO L1 band OS code (1575.42 MHz) receiver
- 2.7 V to 3.3 V power supply
- On-chip LNA
- On-chip PLL including complete VCO
- On-chip IF Band Pass Filter
- 50 dB AGC dynamic range
- SIGN and MAGN outputs
- PLL lock information
- Open / Short Antenna control
- Low power operation 15 mA @ 3.0 Volt
- Supports power-down mode

APPLICATIONS

- Automatic Vehicle Tracking
- Fleet Management
- Security Applications
- Asset Tracking
- Car Telematics / Navigation
- Marine Navigation
- Portable GPS Receiver

GENERAL DESCRIPTION

AST-GPSRF is a high performance, fully integrated, RF front-end chip for down conversion and amplification of GPS and Galileo signals. It has been designed for L1 (1575.42 MHz), C/A GPS band receivers and OS Galileo band receivers.

AST-GPSRF is a superheterodyne receiver, with an on-chip low noise amplifier (LNA), local oscillator, one downconversion IF stage (at 4.092 MHz), an automatic gain controlled amplifier (AGC), an on chip IF band pass filter and a 2-bit analog-to-digital converter (ADC).

The downconverter works with 16.368 MHz reference clock and sampling clock of 16.368 MHz is internally generated.

The downconverter has internal band pass filter, which does not require external calibration.

Antenna connection and open circuit can be sensed and the information is made available.

The chip can be interfaced with any active / passive GPS antenna.

FUNCTIONAL BLOCK DIAGRAM

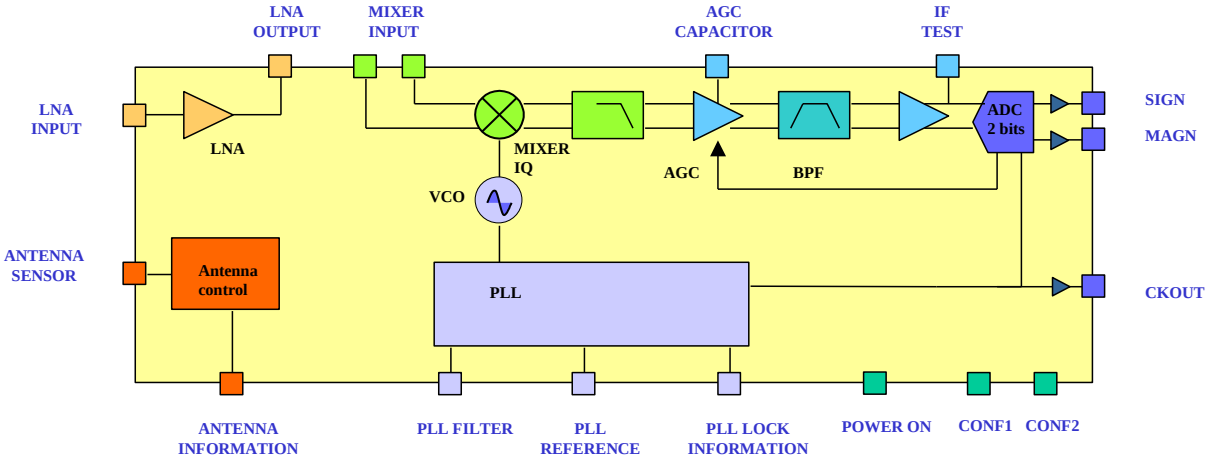

Figure 1. Functional Block Diagram

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REVISION HISTORY
19/06/2017-Revision 1.01

SPECIFICATIONS

Recommended operating conditions: V_{CC} = 2.7 V to 3.3 V, V_{EE} = 0 V, typical is at V_{CC} = 2.7 V, and T_A @ 25°C.

Table 2.

	Parameter	**Conditions**	**Min**	**Typical**	**Max**	**Unit**
	LNA Characteristics	**Refer the LNA matching network section**				
1.1	RF Frequency		1573	1575.42	1577	MHz
1.2	Input Impedance	With matching network		50		Ω
1.3	Input VSWR	With matching network		1.3	2	
1.4	Output impedance	With matching network		50		Ω
1.5	Output VSWR	With matching network		1	2	
	LNA Normal power operation (CONF1 = 0 && CONF2 = X)					
2.1	S21 (Power)	With external matching network	18	21	23	dB
2.2	IP1		-30	-26		dBm
2.3	IIP3	Simulation		-15		dBm
2.4	Noise figure	Simulation		1.5	2	dB
	LNA Low power operation (CONF1 = 1 && CONF2 = 0)					
3.1	S21 (Power)	With external matching network		13		dB
3.2	IP1			-27		dBm
3.3	IIP3	Simulation		-17		dBm
3.4	Noise figure	Simulation		1.8	2.2	dB
	LNA High power operation (CONF1 = 1 && CONF2 = 1)					

4.1	S21 (Power)	With external matching network		19		dB
4.2	IP1			-23		dBm
4.3	IIP3	Simulation		-12		dBm
4.4	Noise figure	Simulation		1.2	2	dB
	Mixer characteristics	**Refer Mixer matching network section (100Ω dual ended)**				
5.1	RF frequency		1573	1575.42	1577	MHz
5.2	LO frequency			1571.328		MHz
5.3	IF frequency			4.092		MHz
5.4	Input impedance	Simulation dual ended		150-j60		Ω
5.5	Input VSWR	Simulation for 100Ω		1.9	2	
5.6	Input impedance	Single ended		50		Ω
5.7	Input VSWR	Single ended for 50Ω			2	
5.8	IIP3	Simulation	-10	-7		dBm
5.9	RF image frequency			1567.23		MHz
5.10	S21 Rejection			15		dBc
5.11	DSB noise figure			15	16	dB
	Reference clock characteristics	**Refer to Reference clock section**				
6.1	Input magnitude level (TCXO input)		0.1	0.4	0.5	V p-p
6.2	Reference frequency			16.368		MHz
6.3	Input load	Simulation		0.5pF parallel with 25KΩ	1pF parallel with 12KΩ	
	VCO Characteristics	**Refer PLL filter section**				
7.1	Nominal frequency	192 times the reference		3142		MHz
7.2	Maximum frequency (VTUNE pin high)		3300			MHz

7.3	Minimum frequency (VTUNE pin low)				3100	MHz
7.4	Phase noise (free running VCO)	@100KHz (Simulation)		-90	-80	dBc / Hz
7.5	Phase noise (closed loop)	With 100kHz loop bandwidth (Simulation)		-90	-80	dBc / Hz
7.6	Spurious (Closed loop) @ reference	Simulation			-40	dBc
7.7	VCO slope	Simulation		0.160		GHz / V
7.8	Current pump charge	Simulation	+/-50	+/-90	+/-150	µA
	IF Characteristics	**Refer AGC / ADC section**				
8.1	IF frequency	With reference frequency		4.092		MHz
8.2	Level at IF_test pin	With R and C network with 50Ω measuring equipment		-55		dBm
8.3	Maximum gain (S21 from mixer input to ADC input)	With AGC active when the AGC amplifier gain is maximum		62		dB
8.4	Minimum gain (S21 from mixer input to ADC input)	With AGC active when AGC amplifier gain is minimum		7		dB
8.5	Noise figure for S21 of 50dB	Simulation			15	dB
8.6	IP1 for S21 maximum	Simulation			-85	dBm
8.7	IP1 for S21 = 30dB	Simulation with Vcamp = 1.6V			-70	dBm
8.8	IP1 for S21 = minimum	Simulation			-30	dBm
	AGC section					
9.1	AGC dynamic range		50	55	65	dB
9.2	AGC slope			60		dB / V
9.3	Magnitude bit duty cycle		23	33	43	%
9.4	AGC band pass upper frequency	With 10nF load on CAMP pin	1	3	10	KHz
9.5	OP1dB	Simulation		2.5		LSB

	IF test point	**With RC network as per AGC / ADC section**				
10.1	Output signal attenuation			34		dB
10.2	Output impedance			250		Ω
	Band Pass Filter CHARACTERISTICS					
11.1	Center Frequency			4.092		MHz
11.2	IF filter bandwidth @ 3dB			4.092		MHz
11.3	IF Filter Ripple	Simulation		2	3	dB
11.4	IF Filter rejection	@ 7 MHz	6			dBc
11.5	IF Filter rejection	@ 8 MHz	15	17		dBc
11.6	IF Filter rejection	@ 14 MHz		20		dBc
	DC levels at Analog pins for various V_{CC}		**2.7**	**3.0**	**3.3**	**V**
12.1	LNAIN pin			0.833		V
12.2	LNAOUT pin		V_{CC}	V_{CC}	V_{CC}	V
12.3	MIXERINP, MIXERINP pins		0.54	0.7	0.85	V
12.4	VTUNE pin			0 / V_{CC}		V
12.5	REF pin		1.35	1.50	1.65	V
12.6	IF_TEST pin	With 10 KΩ resistor		2		V
12.7	CAMP pin			0.5 / V_{CC}		V
12.8	ANT_SENSE pin	No external connection	0	0	0	V
12.9	IBIASBPF pin			0.072		V
	Input CMOS signals (POWER_ON, CONF1, CONF2 pins)					
13.1	V_{IH}		V_{CC}*0.7			V
13.2	V_{IL}				0.3*V_{CC}	V

	Output CMOS signals (SIGN, MAGN, PLL_LOCK, ANT_INFO)					
14.1	V_{OH}		V_{CC}*0.85			
14.2	V_{OL}				0.15*V_{CC}	
14.3	Output drive capacity	Refer AGC / ADC section		5	10	pF
14.4	Skew between CKOUT and SIGN / MAGN	Simulation with 10pF load		1	20	nsec
14.5	Skew between REF and SIGN / MAG	Simulations with 10pF load		18		nsec
	Antenna Connection information	**Refer Antenna control section**				
15.1	ANT_SENSE voltage to detect Antenna connected				V_{CC} – 0.1	V
15.2	ANT_SENSE voltage to detect Antenna disconnection		V_{CC} – 0.5			V
	Current consumption of individual sections					
16.1	VCC_LNA with LNA at normal gain			4		mA
16.2	VCC_LNA with LNA at low gain			2		
16.3	VCC_LNA with LNA at high gain			6		
16.4	VCC_MIX			2		
16.5	VCC_VCO			1.5		
16.6	VCC_IF	At AGC gain of 30dB, 25dB and –25dB	3.2	2.9	2.5	
16.7	VCC_PLL_ADC			2.2mA		
	Total Power					

	consumption					
17.1	Power On mode	2.7 Volt / Conf min / Gain 10 dB		12.5		mA
17.2	Power On mode	3 Volt / Conf nom / Gain 30 dB		16.3		mA
17.3	Standby mode	CKOUT active			1	mA
17.4	Standby mode	CKOUT OFF			50	µA

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating
V_{CC} to V_{EE}[1]	−0.3 V to +3.6 V
Analog I/O Voltage to V_{EE}	−0.3 V to V_{CC} + 0.3 V
Digital I/O Voltage to V_{EE}	−0.3 V to V_{CC} + 0.3 V
RF maximum power	0 dBm (TBC)
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−40°C to +150°C
Maximum Junction Temperature	−40°C to +110°C
Range	

Table 3. ABSOLUTE MAXIMUM RATINGS

[1] V_{EE} = 0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

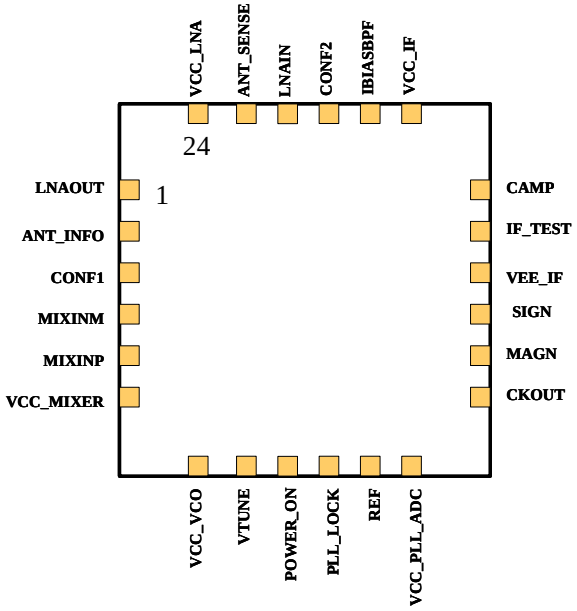

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Pin Type	Input / Output	Description
1	LNAOUT	Analog	Output	LNA RF Signal, (1575.42 MHz)
2	ANT_INFO	Analog	Output	Antenna connection information pin
3	CONF1	CMOS	Input	Configuration pin
4	MIXINM	Analog	Input	Positive MIXER RF Signal, (1575.42 MHz)
5	MIXINP	Analog	Input	Negative MIXER RF Signal, (1575.42 MHz)
6	VCC_MIX	Supply		MIXER Supply
7	VCC_VCO	Supply		VCO Supply
8	VTUNE	Analog		External PLL filter connection
9	POWER_ON	CMOS	Input	Power-On mode pin
10	PLL_LOCK	Analog	Output	PLL LOCK information pin
11	REF	Analog	Input	Reference Clock
12	VCC_PLL_ADC	Supply		PLL / ADC Supply
13	CKOUT	CMOS	Output	Reference frequency
14	MAGN	CMOS	Output	Magnitude Bit Data
15	SIGN	CMOS	Output	Sign Bit Data
16	VEE	Ground		Paddle ground internal connection / redundant with exposed pad

				(paddle)
17	IF_TEST	Analog	Output	IF test
18	CAMP	Analog		Amplitude bit capacitor signal
19	VCC_IF	Supply		IF Supply
20	IBIASBPF	Analog		Internal current source for the BPF
21	CONF2	CMOS	Input	Configuration pin
22	LNAIN	Analog	Input	LNA RF Signal, (1575.42 MHz)
23	ANT_SENSE	Analog	Input	Antenna sense for connection control
24	VCC_LNA	Supply		LNA Supply

Table 4. Pin Function Descriptions

THEORY OF OPERATION

POWER SUPPLIES

The AST-GPSRF uses five different power supply groups as follows:

a. VCC_LNA and VEE_LNA
b. VCC_MIX and VEE_ MIX
c. VCC_VCO and VEE_ VCO
d. VCC_IF and VEE_IF
e. VCC_PLL_ADC and VEE_PLL_ADC

These separate power groups increase isolation between internal components. Each power supply group is externally decoupled by a single low value capacitor for oscillation risk reduction.

Decoupling capacitor used for Power supplies

Component Name	Typical value	Unit
C1 C2	100 10	pF nF

Table 5. Decoupling capacitor used for Power supplies

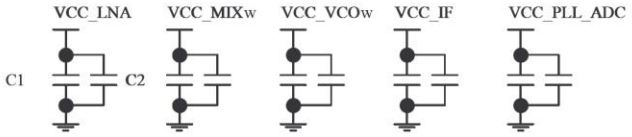

Figure 3. Power supply connections

ISOLATION

Antenna and LNA output
Lna out <->Mixin / VCC_mix <->Vtune / Vtune <->REF / MAG-SIGN <-> LNAIN

MATCHING NETWORK

The RF input has unmatched input impedance. The necessary 50Ω RF external input-matching components must be mounted as close to the RF input as possible. Input and output matching networks provide 50Ω source and load impedance.

LNA MATCHING NETWORK

LNA input is internally biased; therefore, it should be externally ac-coupled.

Tests were made with lumped matching elements, performing maximum power transfer between LNA and input and output. Input matching impedances given in Table 6 are designed for simultaneous input and output matching. Input and output RF signals should be connected to the external devices via a 50Ω line.

External components used for LNA matching

Component Name	Typical value	Unit
C1	NC	pF
C2	100	pF
C3	1.8	pF
L1	4.2	nH
L2	2.2	nH
L3	2.2	nH

Table 6. External components used for LNA matching

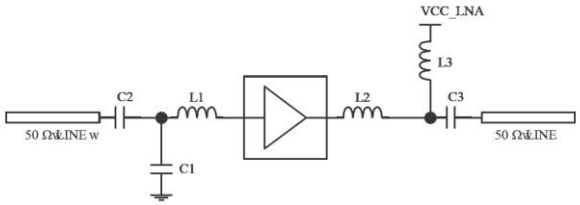

Figure 4. LNA matching network connections

MIXER MATCHING NETWORK

The mixer structure is double-balanced. The local oscillator (LO) input and IF output are fully differential. The RF differential port inputs has a 100Ω matched impedance and is internally biased, so it must be externally ac-coupled.

External components used for Mixer matching

Component Name	Typical value	Unit
C1* C2*	100 100	PF PF

Table 7. External components used for Mixer matching

** Not required if a SAW filter is used or BPF with Internal ac-coupling.*

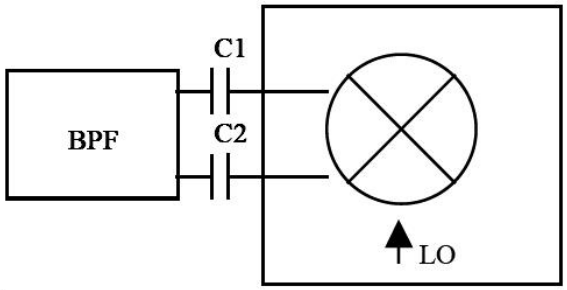

Figure 5. Mixer matching network connection

It is possible to connect a single ended 50Ω Band pass filter to the mixer by connecting the BPF to either MIXINM /

MIXINP and the other mixer input pin to ground using 100pF capacitor.

REFERENCE CLOCK GENERATION

The clock input pin REF is internally biased and must be externally ac-coupled. The PLL works on the rising edge of the TCXO.

External components used for reference input

Component Name	Typical value	Unit
C1	10	nF

Table 8. External components used for reference input

Figure 6. Reference clock connection

PLL FILTER

The PLL generates the local oscillation. It includes a VCO with an on-chip tank circuit, dividers, and a phase detector with external loop filter components. A reference frequency is required for the PLL. The PLL is a second- or a third-order loop, Type 2 for zero frequency error.

The VCO is a monolithic LC voltage controlled oscillator. The divider divides the local oscillator (LO) frequency by 192 before comparing with the reference frequency (REF).

The design of the PLL depends on two criteria: the filtering of the reference frequency signal and the phase noise of the output signal of the PLL. The phase noise of the VCO is filtered by the PLL.

The PLL includes a charge-pump active filter to perform second-order loop. The PLL loop filter components are selected to give a PLL loop bandwidth of approximately 50 / 100 kHz to minimize phase noise.

An additional on-chip LPF (R = 10 KΩ and C = 10 pF) is present in series in the VTUNE command and allows better rejection harmonics of the comparison frequency.

PLL filter is listed in Table 9 and displayed in Figure 7.

External components used for the PLL filter

Component Name	Typical value	Unit
C1	2.7	nF
C2	100	pF
R2	3.3	KΩ

Table 9. External components used for the PLL filter

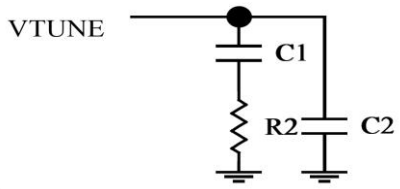

Figure 7. PLL filter connections

AGC / ADC

The internal band pass filter provides the necessary filtering for the system requirement. An auto-calibration is set during the PLL lock phase at each power on and allows to center the filter for the application.

The IFTEST output is used for test purposes only to check the whole RF / IF chain gain. IFTEST pin will output AGC output or ADC input based on ANTENNA_SENSE pin configurations. Refer Antenna Control Pins configuration for more information.

The output impedance of IF TEST pin is around 250Ω.

External components used for IF TEST

Component Name	Typical value	Unit
C1	10	nF
R1	10	KΩ

Table 10. External components used for IF TEST

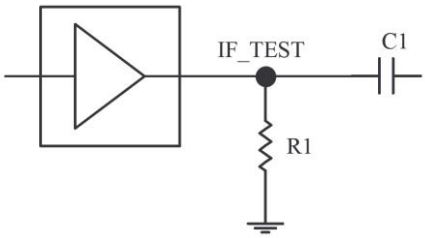

Figure 8.Equivalent IF CHAIN

To maximize the signal-to-noise ratio (SNR) with a 2-bit ADC, the AGC regulation point is fixed at 1σ to activate the amplitude bit 33% of the time. This mean time allows the AST-GPSRF to fix the conversion loss below 0.6 dB.

The CAMP pin can be biased from outside to control the AGC gain.

Table 11 lists the levels of SIGN and MAGN bits with respect to the IF2 magnitude. The data rate of the ADC is dependent on the sampling clock employed in the design.

SIGN and MAGN logic level versus IF2 magnitude level

IF2 Magnitude level	SIGN Logic level	MAGN Logic level
LSB < IF2	1	1
0 < IF2 < LSB	1	0
-LSB < IF2 < 0	0	0
IF2 < -LSB	0	1

Table 11. SIGN and MAGN logic level versus IF2 magnitude level

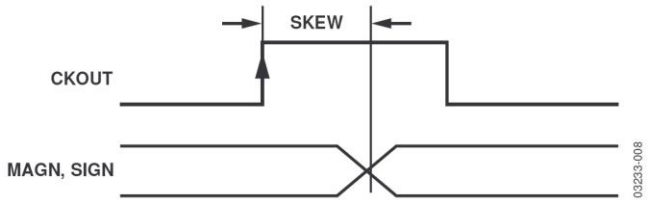

Figure 9. CKOUT to MAGN / SIGN Skew

It is necessary to stabilize the AGC and to set the AGC band-pass to be less sensitive to external strong spurious noise, a capacitor is used on CAMP pin.

External components used with the AGC

Component Name	Typical value	Unit
CAMP	20	nF

Table 12. External components used with the AGC

POWER ON / STANDBY MODE PIN

One digital input pin POWER_ON permits the AST-GPSRF circuit to enter standby mode. The CKOUT can be kept active: see CONF1 and CONF2 pins section.

POWER ON Logic Control Signal

MODE	Logic Level POWER ON
Active	0
Stand By	1

Table 13. POWER ON Logic Control Signal

PLL LOCK PIN

One digital output pin PLL_LOCK permits the AST-GPSRF circuit to provide information on PLL behavior.

PLL_LOCK Logic Control Signal

INFORMATION	Logic Level PLL_LOCK
PLL unlocked	0
PLL locked	1

Table 14. PLL_LOCK Logic Control Signal

When kept at zero bias voltage, the self-tuning of BPF is disabled. This way BPF is at the nominal simulation case. The IBIASBPF pin can be used to tune the BPF.

An external capacitor is required for PLL lock.

External components used for the PLL lock

Component Name	Typical value	Unit
C	10	nF

Table 15. External components used for the PLL lock

CONF1 AND CONF2 PINS

These two digital inputs pins permit AST-GPSRF circuit to increase or decrease chip performance regarding power save consideration or better jammer robustness.

It also can increase the VCO current of about 30% if required.

Configuration Logic Control Signal / power on

MODE: Power ON active (1)	Logic Level CONF1	Logic Level CONF2
Nominal use / ckout clock on	0	0
Nominal use / ckout clock OFF	0	1
Low power use / ckout clock on	1	0
Higher jammer robustness / ckout clock on	1	1

Table 16. Configuration Logic Control Signal / power on

Configuration Logic Control Signal / power off

MODE: Power ON standby (0)	Logic Level CONF1	Logic Level CONF2
Chip powered down / CKOUT active	0	0
Chip fully powered down / CKOUT unactive	0	1

Chip powered down / CKOUT active	1	0
Chip powered down / CKOUT active	1	1

Table 17. Configuration Logic Control Signal / power off

ANTENNA CONTROL PINS

One analog input ANT_SENSE and one digital output ANT_INFO pins permit the AST-GPSRF circuit to check the connection of an active antenna. A drop of 100 mV is necessary to get information of antenna connected.

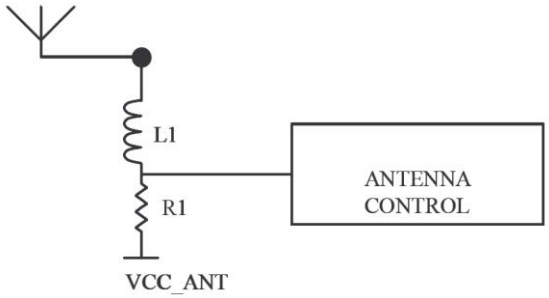

Figure 10.Antenna sensor connections

ANT_INFO Logic Output Signal

INFORMATION	Logic Level ANT_INFO
Antenna disconnected Antenna connected	0 1

Table 18. ANT_INFO Logic Output Signal

R1 should be set to take in account this internal threshold and the active antenna current consumption. The drop is based on the voltage difference between VCC_LNA and the ANT_SENSE pin.

External components used for the antenna sense

Component Name	Typical value	Unit
L1 R1	33 TBD	nH Ω

Table 19. External components used for the antenna sense

DETAILED BLOCK DIAGRAM

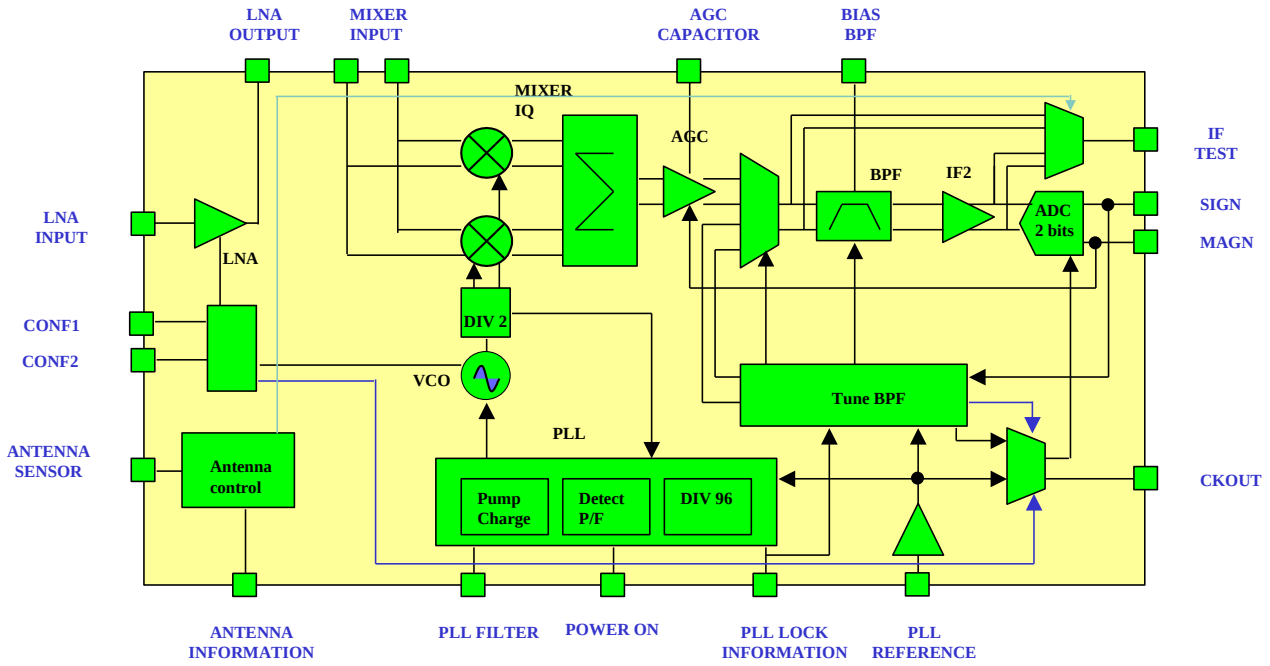

Figure 11. Detailed Block Diagram

CHIP INFORMATION

OUTLINE DIMENSIONS

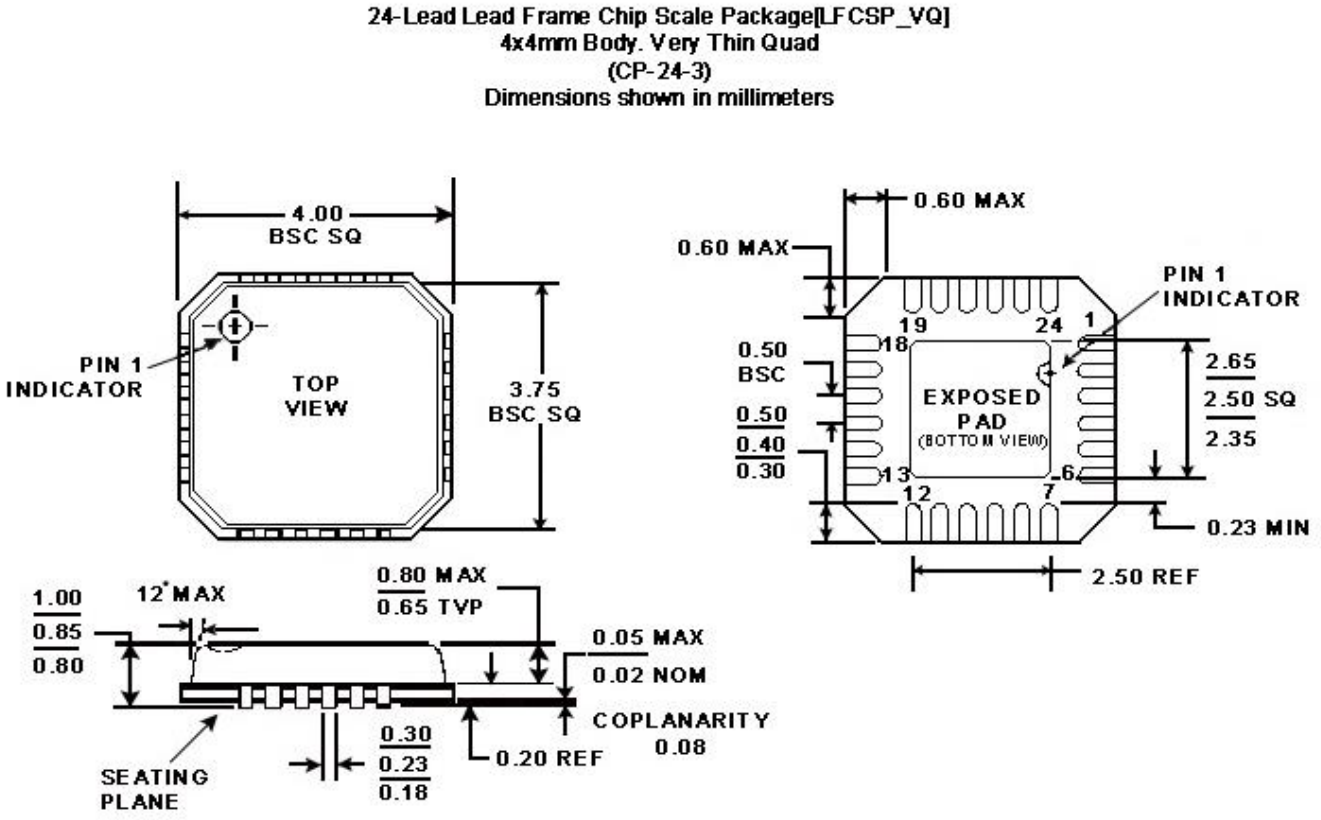

Figure 12. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
Dimensions shown in millimeters

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
AST-GPSRF	3.0 V	−40°C to +85°C	24L LFCSP 4mm x 4mm x 0.85mm Lead Free Package	

Table 20. Ordering Guide

APPLICATION SCHEMATIC

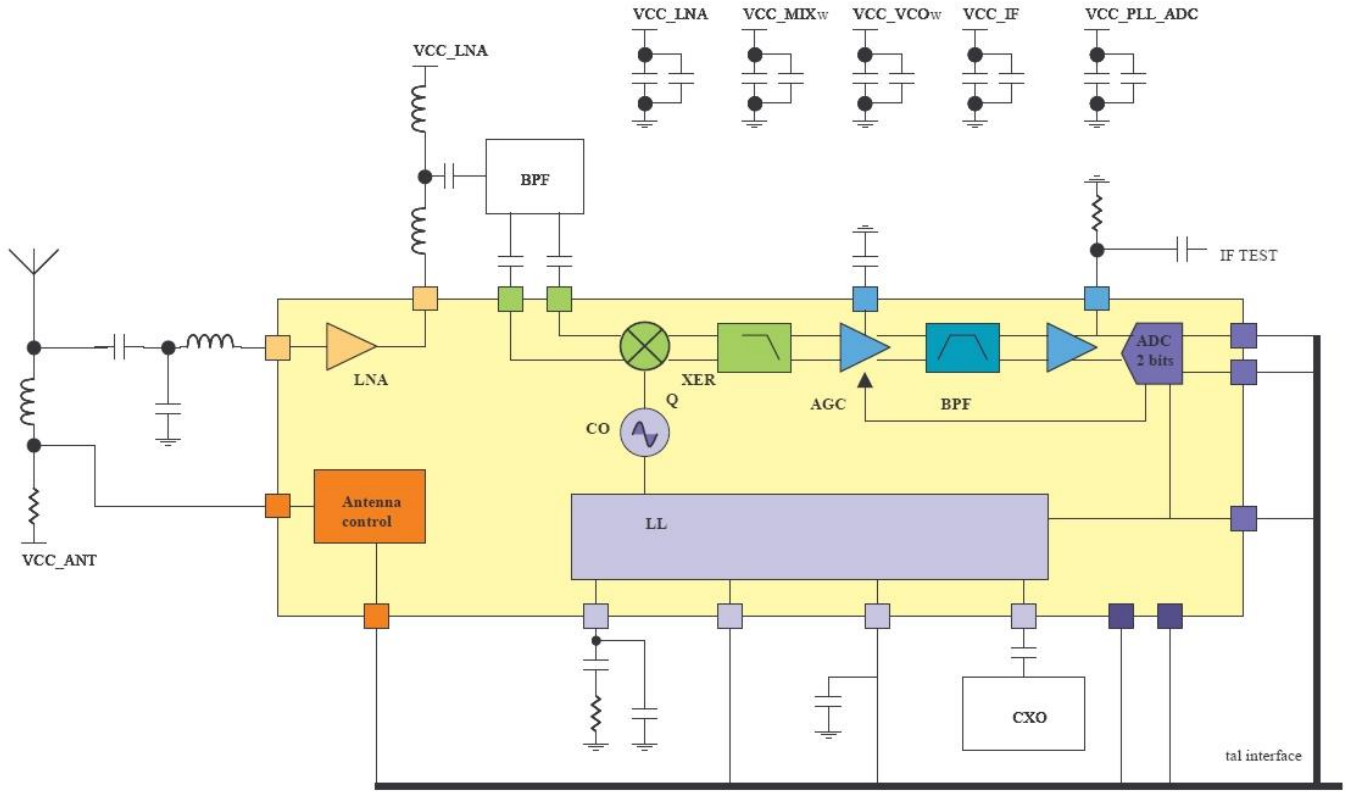

Figure13. Application Schematic