

FEATURES

- Single chip GPS / Galileo downconverter
- GPS L1 band C/A code (1575.42 MHz) receiver
- 2.75 V to 3.3 V power supply
- On-chip LNA
- On-chip PLL including complete VCO
- On-chip IF Band Pass Filter
- 50 dB AGC dynamic range
- SIGN and MAGN outputs
- PLL lock information
- Open/Short Antenna control
- Low power operation 152 mA @ 3.25 Volt
- Supports power-down mode

APPLICATIONS

- Automatic vehicle tracking
- Fleet management
- Asset tracking
- Car telematics/navigation
- Marine Navigation
- Portable GPS receiver

GENERAL DESCRIPTION

AST-GPSRF is a high performance, fully integrated, RF front-end chip for down conversion and amplification of GPS and Galileo signals. It has been designed for L1 (1575.42 MHz), C/A GPS band receivers and OS Galileo band receivers.

AST-GPSRF is a superheterodyne receiver, with an on-chip low noise amplifier (LNA), local oscillator, one downconversion IF stage (at 4.092 MHz), an automatic gain controlled amplifier (AGC), an on chip IF band pass filter and a 2-bit analog-to-digital converter (ADC).

The down converter works with 16.368MHz reference clock and sampling clock of 16.368MHz is internally generated.

The down converter has internal band pass filter, which does not require external calibration.

Antenna connection and open circuit can be sensed and the information is made available.

The chip can be interfaced with any active/passive GPS antenna.

FUNCTIONAL BLOCK DIAGRAM

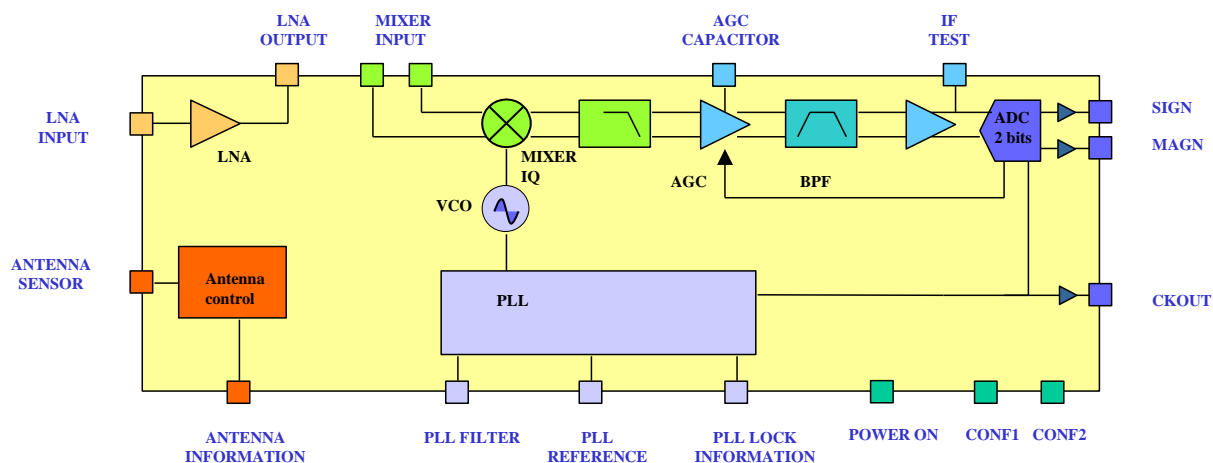


Figure 1. Functional Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

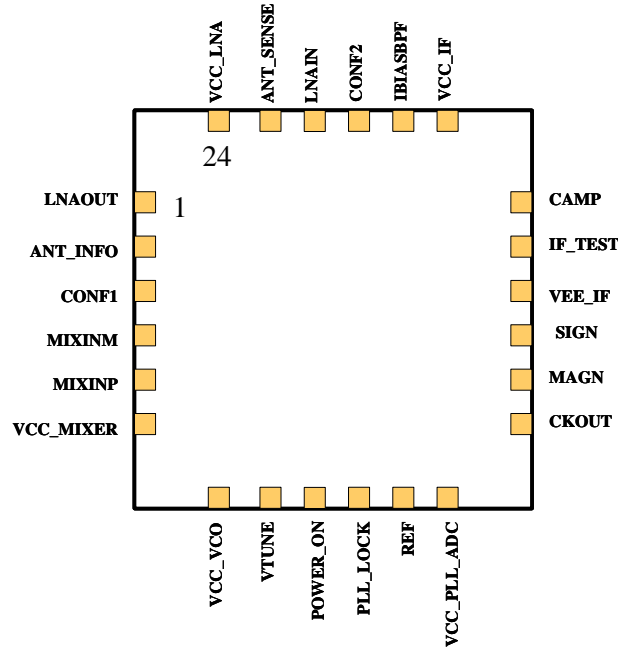


Figure 2. Pin Configuration

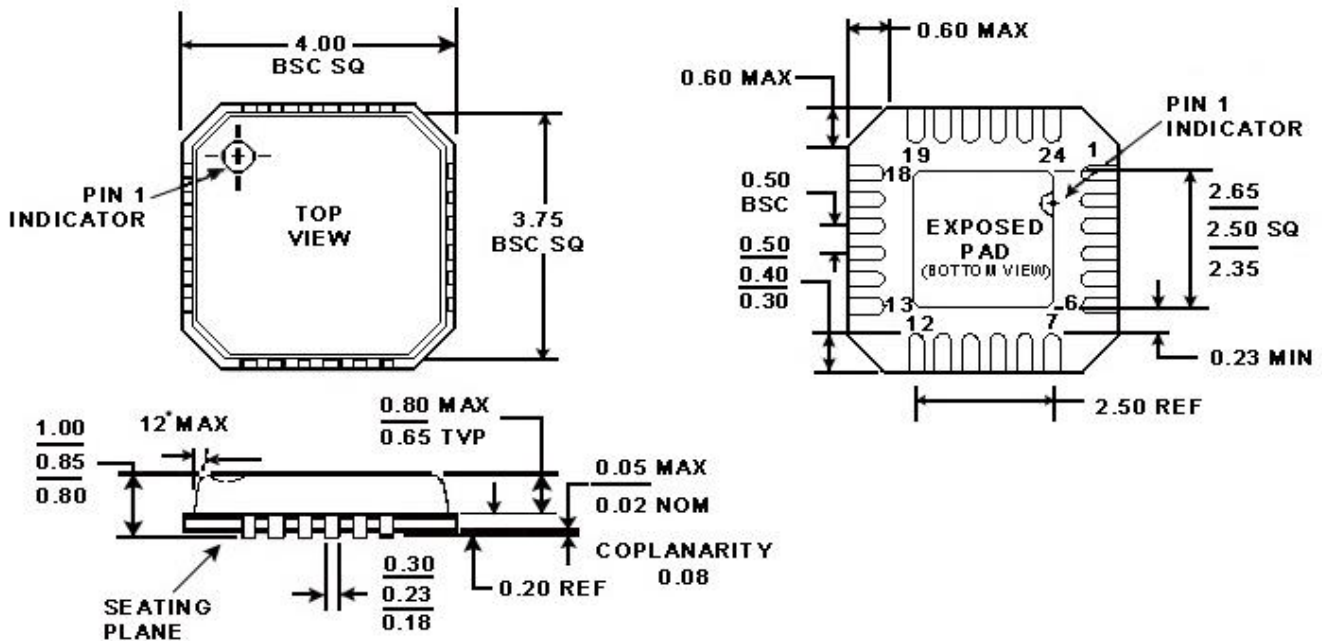
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Pin Type	Input / Output	Description
1	LNAOUT	Analog	Output	LNA RF Signal, (1575.42 MHz)
2	ANT_INFO	Analog	Output	Antenna connection information pin
3	CONF1	CMOS	Input	Configuration pin
4	MIXINM	Analog	Input	Positive MIXER RF Signal, (1575.42 MHz)
5	MIXINP	Analog	Input	Negative MIXER RF Signal, (1575.42 MHz)
6	VCC_MIX	Supply		MIXER Supply
7	VCC_VCO	Supply		VCO Supply
8	VTUNE	Analog		External PLL filter connection
9	POWER_ON	CMOS	Input	Power-On mode pin
10	PLL_LOCK	Analog	Output	PLL LOCK information pin
11	REF	Analog	Input	Reference Clock
12	VCC_PLL_ADC	Supply		PLL/ADC Supply
13	CKOUT	CMOS	Output	Reference frequency
14	MAGN	CMOS	Output	Magnitude Bit Data
15	SIGN	CMOS	Output	Sign Bit Data
16	VEE	Ground		Paddle ground internal connection / redundant with exposed pad (paddle)
17	IF_TEST	Analog	Output	IF test
18	CAMP	Analog		Amplitude bit capacitor signal
19	VCC_IF	Supply		IF Supply
20	IBIASBPF	Analog		Internal current source for the BPF
21	CONF2	CMOS	Input	Configuration pin
22	LNAIN	Analog	Input	LNA RF Signal, (1575.42 MHz)
23	ANT_SENSE	Analog	Input	Antenna sense for connection control
24	VCC_LNA	Supply		LNA Supply

Table 1. Pin Function Descriptions

PACKAGE INFORMATION

24-Lead Lead Frame Chip Scale Package[LFCSP_VQ]
4x4mm Body. Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 3. Package information

ORDERING GUIDE

Model	Operating Voltage	Temperature Range	Package Description	Package Option
AST-GPSRF	3.0 V	-40°C to +85°C	24L LFCSP 4mmx4mmx0.85mm, Lead free package	

Table 2. Ordering Guide

APPLICATION SCHEMATIC

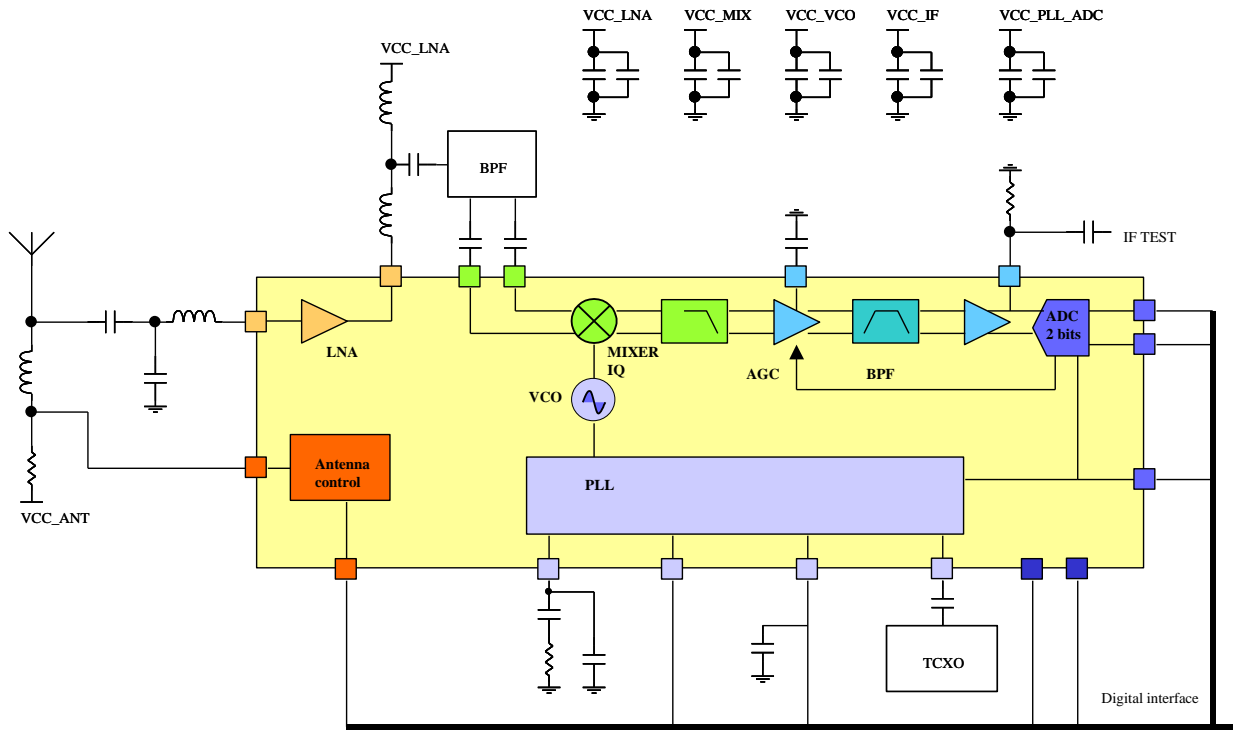


Figure 4. Example application schematics