Technical Data

SST-200

GNSS Hardware Accelerator

FEATURES

- High performance GNSS Baseband Correlator
- 1.7K correlators for enhanced sensitivity and faster time to first fix
- Easily mates with GNSS RF and Application processor
- Supports fast time to fix and superior sensitivities in acquisition and tracking
- Accurate time output
- SPI protocol for data exchange with application processor
- Small footprint of 5mm x 5mm (TQFN)
- Supports industrial temperature range
- ROHS compliant

APPLICATIONS

SST-200 is a miniature high performance GNSS correlator that can be used to realize a variety of GNSS modules and solutions.

The main segments where SST-200 is an ideal choice is

- GNSS modules
- Base station timing Solutions
- Automotive applications

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FUNCTIONAL BLOCK DIAGRAM

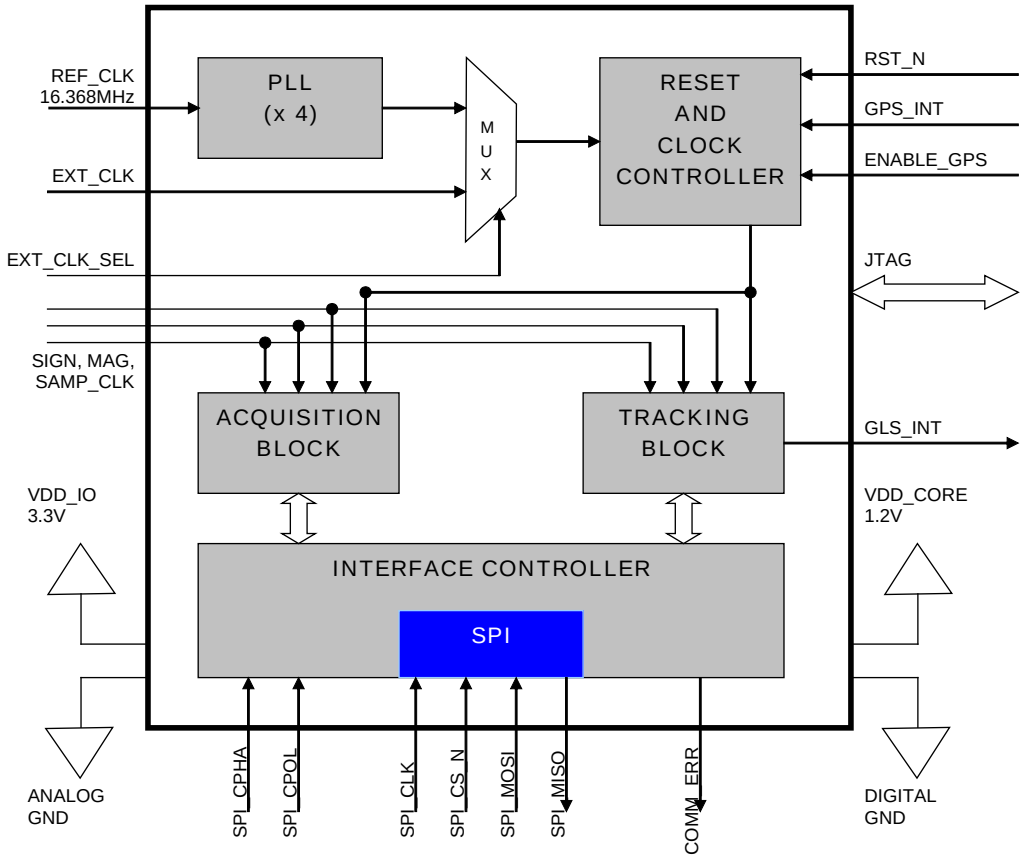

Figure 1: Block Diagram of SST-200

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REVISION HISTORY

January 2017-Revision 1.0

GENERAL DESCRIPTION

SST-200 is a high performance GNSS correlator ASIC aimed at diverse applications in Automotive, Consumer Electronics, Infrastructure, Healthcare and Industrial market segments.

SST-200 interfaces with a generic GNSS RF front end (for example, AST-GPSRF or AST-GLSRF from Accord Software and Systems Pvt. Ltd.).

Programming interface is made available over the SPI interface which allows the firmware to program the satellites in acquisition or tracking. SST-200 provides the correlation results over the SPI interface to any generic processor.

SST-200 integrates several functional blocks such as Acquisition block, Tracking block, PLL, Reset and Clock controller and an Interface block in a small 5mm x 5mm TQFN package.

The key functional blocks are explained below.

GNSS BASEBAND

At the heart of the SST-200 is the GNSS baseband. This is a 14-channel correlator capable of interfacing with a standard front-end. The in-built correlators are designed to provide the maximum sensitivity and the shortest time to acquisition, thereby ensuring that the chip delivers unmatched performance. The GNSS baseband is seamlessly connected to any processing core through the SPI bus to exchange the programming parameters and the correlation results. The GNSS firmware running on the processor runs the tracking loops and navigation algorithms.

The GNSS baseband in turn has 2 blocks:

- Acquisition block
- Tracking block

The Acquisition block consists of 1.7K correlators to search in both time and frequency domains. The large number of correlators ensure faster time to first fix (TTFF) even at lower sensitivities.

The Tracking block finely tracks the code and carrier dopplers and provides measurements to the firmware to form the navigation solution.

The code and carrier generators are separately provisioned for Acquisition and Tracking blocks.

PLL

The PLL block takes in a reference clock of 16.368MHz and generates an ‘x4’ clock to run the acquisition and tracking blocks.

It is possible to bypass the output from the PLL by supplying the desired clock directly to all the blocks.

RESET & CLOCK CONTROLLER

The Reset block accepts an external active low reset input and resets all the internal blocks.

The Clock Controller block sets the operational state of the chip. The block senses the selection on one of the pins and configures the chip as either GPS or GLONASS correlator.

This block accepts an external measurement latch interrupt pulse to synchronize its measurements as part of a bigger multi-constellation system.

INTERFACE CONTROLLER

The Interface Controller implements an SPI port for communication with an external processor. The SPI interface is made of 4 lines – CLK, CS, MOSI and MISO. In addition, two control lines to select the phase and polarity of the clock is also provided. In order to detect possible errors in communication, an output line is provided to flag off such an event.

The SPI data transfer can work at high speeds of up to 40 MHz.

APPLICATION CIRCUIT

A typical application block schematic is shown in Figure 2. The configurations of the various pins correspond to the SST-200 being used as a GLONASS Correlator. The SST-200 is interfaced to AST-GLSRF, a GLONASS RF front-end ASIC from Accord Software and Systems. It is interfaced to a standard processor which supports full-duplex SPI interface and has sufficient processing power to run the GLONASS baseband and navigation algorithms.

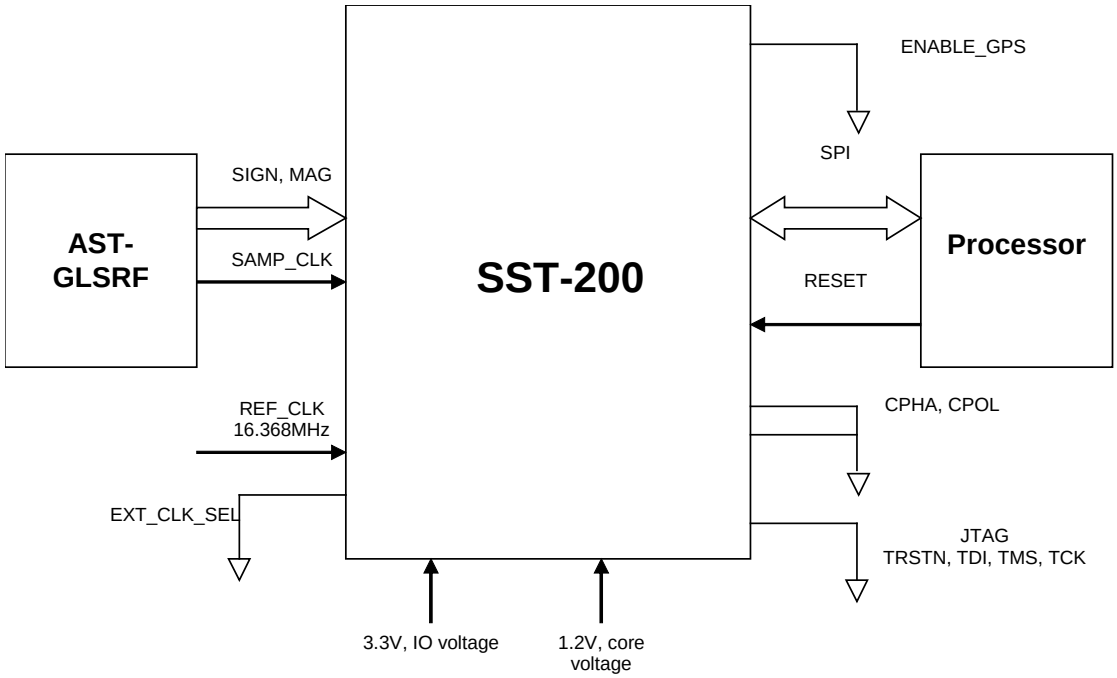


Figure 2: Application Block Schematic

SPECIFICATIONS

ENVIRONMENTAL SPECIFICATIONS

Table 1: Environmental Specifications

Parameter	Conditions	Min	Nominal	Max	Units
Operating Temperature		-40	+25	+85	C
Junction Temperature		-40	+25	+125	C
ESD	JS-001-2010			> +/- 2KV	
	JESD 22-C101			> +/- 500V	
MSL	JESD 22-A 113 J-STD-020		3		

ELECTRICAL CHARACERISTICS

Table 2: Electrical Characteristics

Parameter	Test Conditions	Min	Typical	Max	Unit
Internal Supply Voltage		1.08	1.2	1.32	Volts
External Supply Voltage		3.0	3.3	3.6	Volts
High Level Input Voltage (VIH)		2.0		3.6	Volts
Low Level Input Voltage (VIL)		-0.3		+0.8	Volts
High Level output Voltage (VOH)		2.4			Volts
Low Level output Voltage (VOL)				0.4	Volts
High Level output Current (IOH) @ VOH (min)		10.2	19.9	32.2	mA
Low Level output Current (IOL) @ VOL (max)		7.2	11.8	17.1	mA
Input capacitance Output capacitance		5 15			pf

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute Maximum Rating

Table 3: Absolute Maximum Rating

Parameter	Rating
Internal Supply Voltage	1.32 V
External I/O Supply voltage	3.6 V
Load Capacitance	20 pf
Storage temperature range	-65 ^{0}C to 150 ^{0}C
Junction Temperature Under bias	-40 ^{0}C to 125 ^{0}C

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

SST-200 pin definitions are listed in Table 9.

Functional Pin Description

Table 4: Functional Pin Description

Port Name	Description	Default Value	Pull Up (PU) / Pull Down (PD)	I/O
SIGN	Bit 1 of IF sample from the GPS or GLONASS RF. When using AST-GPSRF or AST-GLSRF, this pin is driven on the rising edge of SAMP_CLK		NA	I
MAG	Bit 0 of IF sample from the GPS or GLONASS RF. When using AST-GPSRF or AST-GLSRF, this pin is driven on the rising edge of SAMP_CLK		NA	I
SAMP_CLK	ADC Clock output from the GPS or GLONASS RF. 16.368MHz from AST-GPSRF (ENABLE_GPS = 1) and 26.598MHz from AST-GLSRF (ENABLE_GPS = 0)		NA	I
REF_CLK	16.368Mhz Clock to generate the system clock		NA	I
GLS_INT	A 10ms interrupt to the processor. Generated using the GLONASS RF sampling clock (SAMP_CLK)	0	NA	O
GPS_INT	A 10ms interrupt to the SST-200. Used to synchronize the measurement latching across several correlators		NA	I
RST_N	An active low Reset input		PU	I
EXT_CLK	Externally supplied system clock Should be 65.472 MHz, CMOS (0 to 3.3V)			I
EXT_CLK_SEL	Selection of the source of the system clock 0: Internal clock is selected 1: Clock supplied through EXT_CLK pin is selected			I
ENABLE_GPS	Selection of GPS or GLONASS correlation 0: GLONASS correlator 1: GPS correlator		PU or PD	I
SPI_CLK	Clock supplied by SPI master for SPI communication			I
SPI_CS_N	Active low SPI chip select		PU	I
SPI_MOSI	Master Output Slave Input			I
SPI_MISO	Master Input Slave Output	0		O
SPI_CPOL (Clock polarity selection) & SPI_CPHA (Clock phase selection)	At SPI_CPOL=0 the base value of the clock is zero • For SPI_CPHA=0, data are read on the clock's rising edge and data are changed on a falling edge. • For SPI_CPHA=1, data are read on the clock's falling edge and data are changed on a rising edge.			I

	At SPI_CPOL=1 the base value of the clock is one (inversion of SPI_CPOL=0) • For SPI_CPHA=0, data are read on clock's falling edge and data are changed on a rising edge. • For SPI_CPHA=1, data are read on clock's rising edge and data are changed on a falling edge.			I
TRSTN	JTAG reset Acts as a test pin during test mode		PD to GND through 0e	I
TDI	JTAG data in Acts as a test pin during test mode		PD to GND through 0e	I
TDO	JTAG data out Acts as a test pin during test mode	0		O
TMS	JTAG mode select Acts as a test pin during test mode		PD to GND through 0e	I
TCK	JTAG clock Acts as a test pin during test mode		PD to GND through 0e	I
COMM_ERR	Communication error during SPI data transfer. It is asserted for any error in checksum or header of the data packet 0: No error 1: Error The line is held at logic ‘1’ for a duration of 500ms	0		O

TIMING SPECIFICATIONS

GNSS Signals

Table 5: GNSS Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
SIGN	0	12	-	-
MAG	0	12	-	-
$tCLK_{GPS}$ (SAMP_CLK)	16.368MHz			
$tCLK_{GLONASS}$ (SAMP_CLK)	26.598MHz			
tCLK (SYS_CLK)	65.472MHz (4 x $tCLK_{GPS}$)			

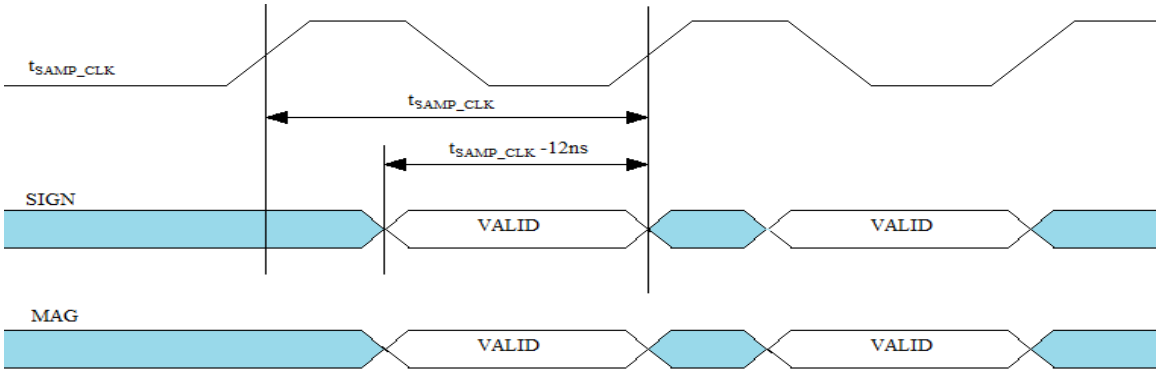


Figure 3: GNSS signals Timing Diagram

SPI Signals

Table 6: SPI Signals

Signals	Input Delay (ns)		Output Delay (ns)	
	Min	Max	Min	Max
SPI_MOSI	1.6	18.4	1	14
SPI_MISO	-1.5	9.5	0	10
SPI_CS_N	1.5	10	-	-
tCLK (SPI_CLK)	22.5MHz			

Clock and Reset Timing

Table 7: Clock and Reset Timing

Parameter	Minimum	Maximum	Unit
tCKIN		61	ns
tCKINL CLKIN Low Pulse		31	ns
tCKINH CLKIN High Pulse		31	ns
tWRST RESET Asserted Pulse Width Low	5		us

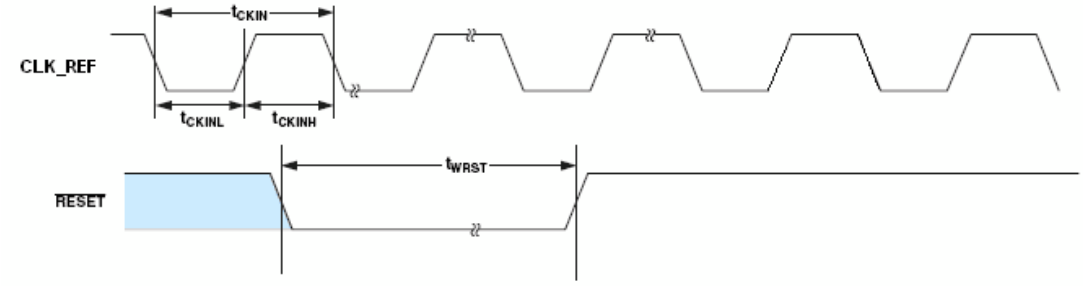


Figure 4: Clock and Reset Timing

Serial Peripheral Interface (SPI) Port—Slave Timing

Below Table and Figure, describe SPI port slave operations.

Serial Peripheral Interface (SPI) Port—Slave Timing

Table 8: Serial Peripheral Interface (SPI) Port—Slave Timing

Parameter	V_{DDEXT} = 1.8V LQFP/PBGA Packages Min	Max	V_{DDEXT} = 1.8V MBGA Package Min	Max	V_{DDEXT} = 2.5V/3.3V All Packages Min	Max	Unit
Timing Requirements							
t_{SPICHS} Serial Clock High Period	$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		ns
t_{SPICLS} Serial Clock Low Period	$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		ns
t_{SPICLK} Serial Clock Period	$4t_{SCLK}$ - 1.5		$4t_{SCLK}$ - 1.5		$4t_{SCLK}$ - 1.5		ns
t_{HDS} Last SCK Edge to $\overline{SPISS}$ Not Asserted	$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		ns
t_{SPITDS} Sequential Transfer Delay	$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		ns
t_{SDSCI} $\overline{SPISS}$ Assertion to First SCK Edge	$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		$2t_{SCLK}$ - 1.5		ns
t_{SSPID} Data Input Valid to SCK Edge (Data Input Setup)	1.6		1.6		1.6		ns
t_{HSPID} SCK Sampling Edge to Data Input Invalid	1.6		1.6		1.6		ns
Switching Characteristics							
t_{DSOE} $\overline{SPISS}$ Assertion to Data Out Active	0	10	0	9	0	8	ns
t_{DSDHI} $\overline{SPISS}$ Deassertion to Data High Impedance	0	10	0	9	0	8	ns
t_{DDSPID} SCK Edge to Data Out Valid (Data Out Delay)	0	10	0	10	0	10	ns
t_{HDSPID} SCK Edge to Data Out Invalid (Data Out Hold)	0	10	0	10	0	10	ns

Serial Peripheral Interface (SPI) Port—Slave Timing

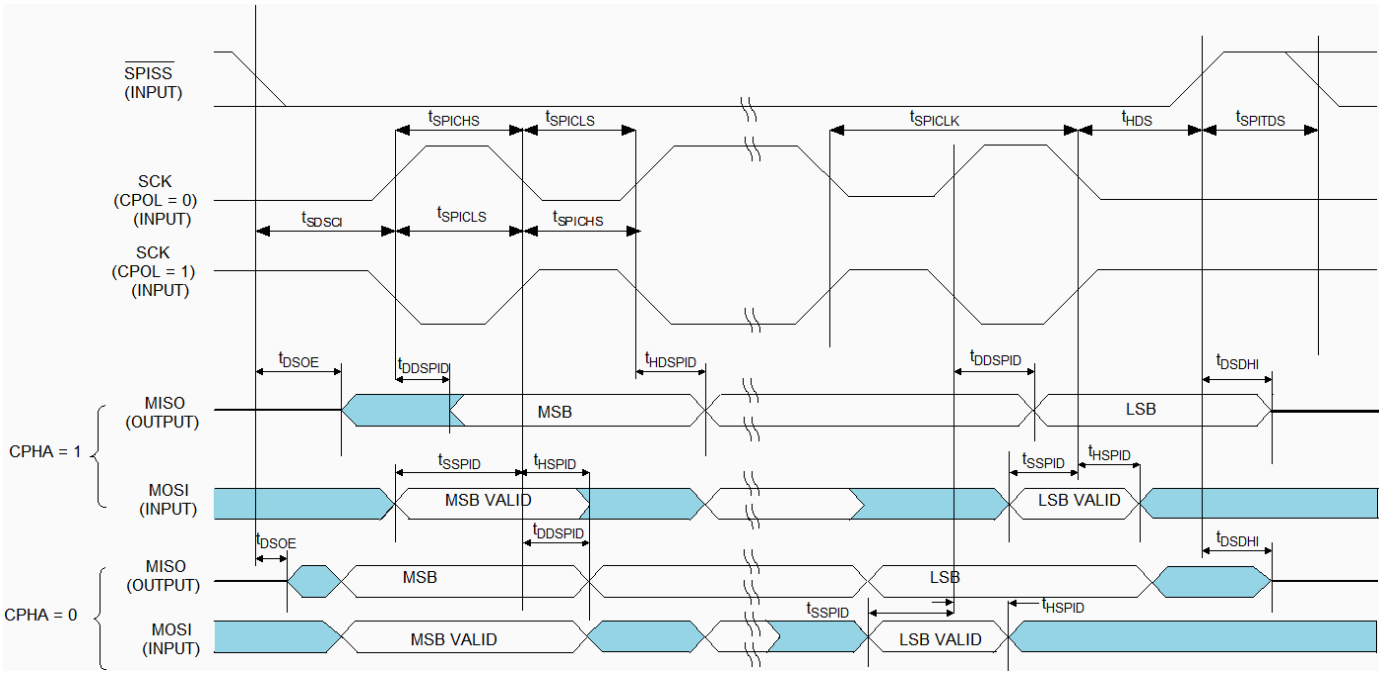


Figure 5: Serial Peripheral Interface (SPI) Port—Slave Timing

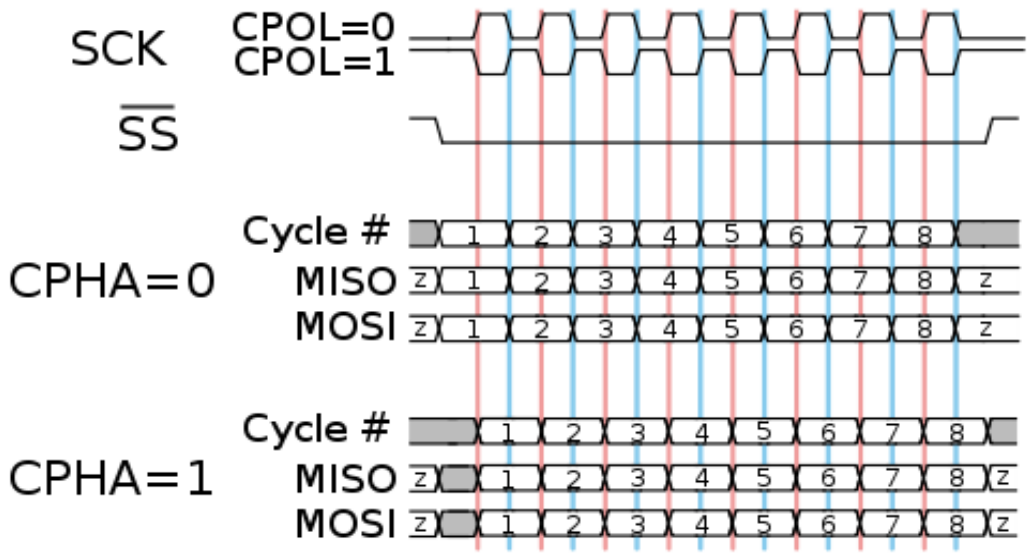


Figure 6: SPI Modes-Timing Diagram

40-LEAD TQFN PIN ASSIGNMENT

Table 9: 40- Lead TQFN Pin Assignment

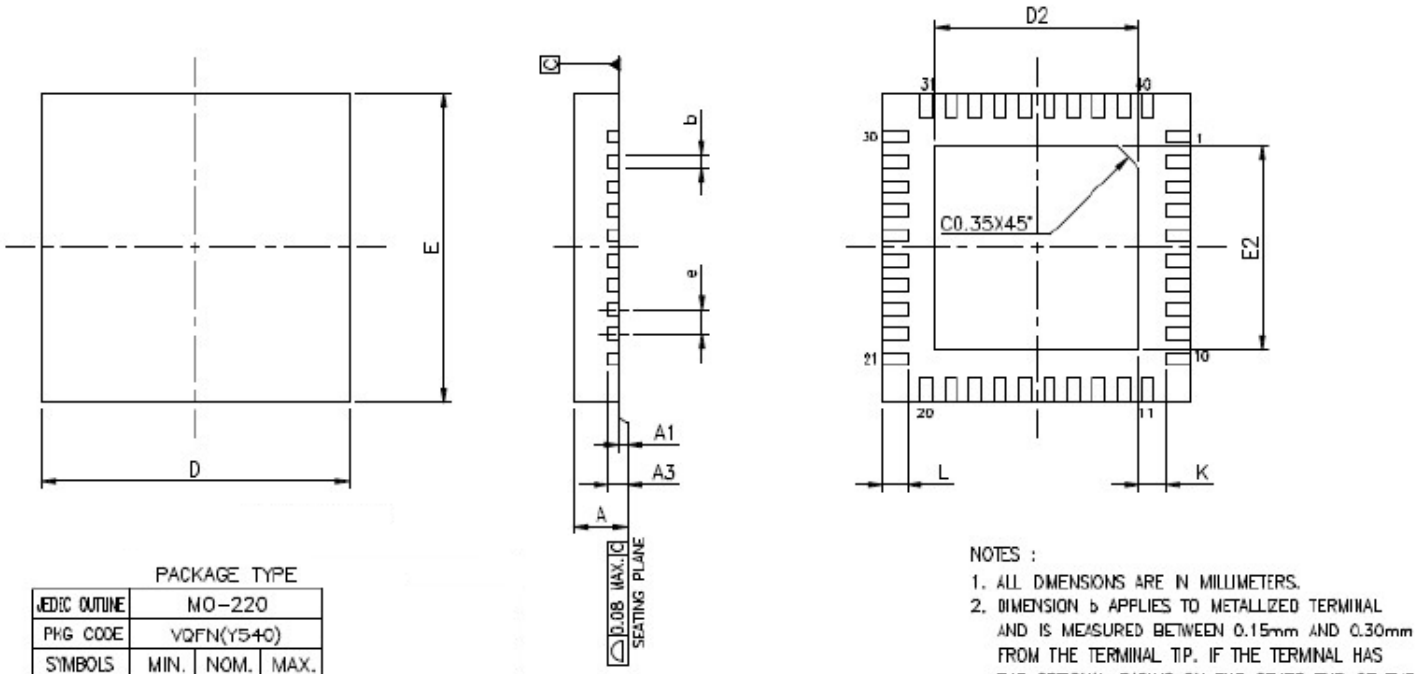
Ball No	Signal Name
1	SIGN
2	MAG
3	SAMP_CLK
4	GND
5	EXT_CLK
6	EXT_CLK_SEL
7	VCC_1V2
8	GND
9	REF_CLK
10	AVDD
11	AVSS
12	VCC_1V2
13	GND
14	TRSTN
15	TDI
16	TDO
17	TMS
18	TCK
19	GND
20	VCC_1V2
21	SPI_CPOL
22	SPI_CPHA
23	VCC_3V3
24	GND
25	SPI_MISO
26	VCC_1V2
27	GND
28	SPI_CLK
29	SPI_CS_N
30	SPI_MOSI
31	GND
32	COMM_ERR
33	GPS_INT
34	RST_N
35	GLS_INT
36	GND
37	VCC_3V3
38	ENABLE_GPS
39	VCC_1V2
40	GND

OUTLINE DIMENSIONS

The Package is 5mm x 5mm. Dimensions in below Figure-7 with 40-pin TQFN are shown in millimeters.

SURFACE MOUNT DESIGN

The following table is provided as an aide to PCB design. For industry-standard design recommendations, refer to IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standard



PACKAGE TYPE

JEDIC OUTLINE	MO-220		
PKG CODE	VQFN(Y540)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.15	0.20	0.25
D	5.00 BSC		
E	5.00 BSC		
e	0.40 BSC		
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

	E2			D2			L			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
153X153 MIL	3.20	3.30	3.35	3.20	3.30	3.35	0.35	0.40	0.45	V	X	N/A
2 159X159 MIL	3.69	3.79	3.84	3.69	3.79	3.84	0.25	0.30	0.35	V	X	N/A

Figure 7: 40L TQFN

ASSEMBLY INSTRUCTIONS

The SST-200 chip should be assembled using ROHS process.

ORDERING GUIDE

Table 10: Ordering Guide

Model	Temperature Range	Package Description	Operating Voltage
SST-200	-40 ^{0}C to +85 ^{0}C	40L TQFN 5mm x 5mm x 0.85mm	1.2 V (core), 3.3 V I/O