Software-Aided Sequential Multi-Tap Correlator for Fast Acquisition

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ABSTRACT

The requirement for GPS receivers with low Time To First Fix (TTFF) is increasing with the deployment of new standards like E911. Mean Acquisition Time (MAT) determines the TTFF in GPS receivers. In this paper we analyze a scheme called Sequential Muti-Tap correlator, which reduces MAT by an order of magnitude compared to a serial search correlator, without increasing the hardware significantly.

The Sequential Multi-Tap (SMT) correlator is compared with other fast acquisition schemes with respect to various benchmark parameters like MAT, gate density, TTFF etc. and shown to outperform other approaches in a standard GPS receiver application. The SMT correlator scheme tends to be a potential candidate for low gate count and low power IP integrations.

I. INTRODUCTION

The growth and the regular use of GPS applications are demanding significant improvement in the performance of the GPS receivers.The E911 standard implementation for mobile phones has also prompted basic structure of these receivers. These requirements may be broadly classified as

- ➢ Increased position availability
- ➢ Reduced power consumption
- ➢ Reduced form factor

The reliability may be improved by improving algorithms and by integration with other navigational aids such as dead reckoning sensors and/or other radio-location aids (like mobile phones). Increasing the solution update rate can increase the position availability. Power consumption can be reduced by improved semiconductor technology and new architectural and logical improvements in the receivers. Smaller form factor may be achieved through increased on-chip integration and by integrating several functionalities in the same hardware configuration. Better semiconductor technology provides means for reducing the size to a minimum. These requirements are aided by an improved Time-To-First-Fix (TTFF) performance of the receiver.

The average time spent in acquisition of a visible satellite signal (Mean Acquisition Time) determines the TTFF. Hence reducing the MAT to a minimum is a direct way of minimizing the TTFF. However the MAT is highly dependent on the search strategy and sensitivity of the

receivers. Serial search schemes, traditionally used, give out less scope for improvement of these parameters. The advanced semiconductor technology provides scope for parallel search of code and frequency. This enables refining of the algorithms to cater for multiple tap correlator. With multiple tap correlator significant savings in processing may be achieved by eliminating some redundant computations as described later in the paper.

Several techniques have been discussed in literature to improve the acquisition time of a GPS receiver [13, 14, 8]. Fast Acquisition receivers normally use circular convolution for performing the correlation. Since the incoming and local code sequences are of finite duration, this is achieved by frequency domain multiplication [13]. The implementation feasibility and reduction in computational complexity have been studied in [16, 17]. Nevertheless there are some disadvantages with the approach mentioned in these papers. First, the hardware complexity is increased due to FFT blocks. Second, the processing resource used for acquisition cannot be reused for tracking. Hence for tracking, a serial correlator is required separately. These drawbacks make these schemes unusable for low cost applications.

In this paper we propose a correlator scheme to reduce the MAT. The proposed method employs sequential architecture for multiple channels. In a single correlator block, multiple time cells are searched simultaneously. Combining sequential processing of channels with that of multiple time cell search in each channel results in lower hardware requirements in implementation compared to parallel channel processing that employs multiple time cell searches in each channel.

II. GPS SIGNAL ACQUISITION

Brief GPS signal characteristics for C/A code [3] is summarized in the Table-1.

Frequency Band	L1
Frequency	1575.42MHz
Minimum power at 0dBi receiver antenna	-160dBW
Wavelength	19.03cm
Code length	1023
Chipping Rate	1.023MHz
Navigation data rate	50bps
Navigation data modulation	BPSK

Table 1 GPS Signal Characteristics

The GPS signal at the receiving antenna (assuming no multipath) can be expressed as

$$r(t) = \sum_{k=1}^{K} \sqrt{2S_k} d_k(t) c_k(t + \tau_k T_c) \cos(\omega_0 t + \omega_k t + \theta_k) + n(t)$$

where K is the number of GPS satellites in view. For the kth satellite, S_k is the received signal power from it, $d_k(t)$ is the navigation data, $c_k(t)$ is the code sequence, τ_k is the time delay, θ_k is the random phase ω_k is the doppler angular frequency, T_c is the chip duration, ω_0 is the carrier angular frequency, $n(t)$ represents the AWGN with two sided power spectral density $N_0 / 2$ (W/Hz).

The input to the GPS correlator is a digitized and sampled IF signal. The 50 bps navigation data is extracted from this signal for each visible satellite. For each satellite, the receiver has to synchronize the local code replica and doppler frequency with the received signal. Acquisition is a coarse synchronization process that provides approximate delay and frequency estimates.
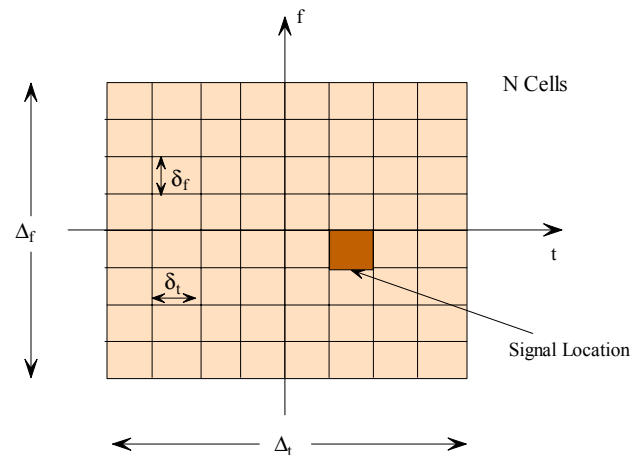
A. RECEIVER SEARCH SPACE

Figure 1: Receiver Search Space (from [9])

Acquisition process is a two dimensional search: one search is within time uncertainty (Δ_t) and the other within the frequency uncertainty (Δ_f). This may be represented as shown in Figure-1. In the figure, δ_t and δ_f represent the search step sizes in time and frequency respectively. δ_t is expressed in fraction of a chip and δ_f is in Hertz. These step sizes are chosen to allow code and carrier tracking loops to lock on to the GPS signal (fine synchronization). Typically for a receiver used in

moderate dynamics applications, $\delta_t = 1/2$ and $\delta_f = 250$Hz. The total number of search cells is

$$N = \frac{\Delta_f \cdot \Delta_t}{\delta_f \cdot \delta_t}$$

Parallel frequency search reduces the total number of search cells. For non-overlapping M_C parallel frequency bins, the number of searches required is

$$N' = \frac{N}{M_C}$$

If the search has to cover the complete frequency ambiguity, then $M_C = \Delta_f / \delta_f$.

The acquisition process consists of testing each cell for the presence of signal. This is achieved by correlating the local replica C/A code of all satellites with the received signal, for all possible time shifts. If the test statistic exceeds the threshold, then it is decided that the particular satellite is present and a transition to tracking process is initiated with the approximate time delay and frequency estimates. Otherwise, if the test statistic falls below the threshold for all the cells, then it is declared that the particular satellite is not in view and next satellite is selected for search process. The time spent in an unoccupied cell before continuing with the next cell is

termed as "dwell time". Total time for searching one satellite would be $N \cdot \tau_D$ where τ_D is the dwell time.

Frequency search can be accomplished using step by step frequency bin search or through Discrete Fourier Transform. The Integrate and Dump (ID) filter determines the doppler ambiguity that can be accommodated. For example, integrate and dump duration of 15.625us implies a frequency window of 64 KHz (without considering the effect of sinc type response of the ID filter). Depending on the a priori information about the satellite orbit parameters and the local clock characteristics, the doppler ambiguity can range from few KHz (moderately stable clock) to tens of KHz (for lower stability clock).

B. GENERIC CORRELATOR STRUCTURE

The conventional correlator structure [11] is shown in Figure-2. The received signal is multiplied by both inphase and quadrature components of the locally generated carrier. The resultant is multiplied with the locally generated code of a particular chip shift. An Integrate and Dump filter follows the code mixing. Both inphase and quadrature correlation values for a chip shift are then used for envelope detection. The acquisition decision variable is then compared against a threshold.
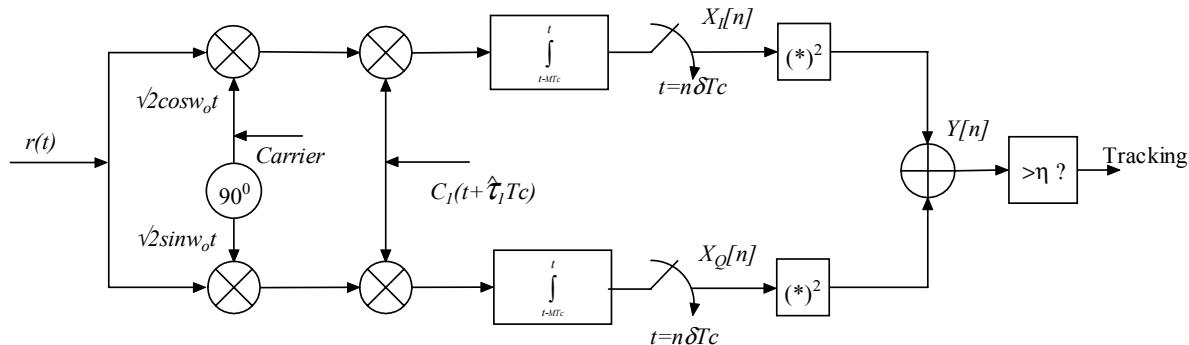

Figure 2: Generic Correlator Structure

The acquisition decision variable $Y[n]$ is computed as $X_I[n]^2 + X_Q[n]^2$. If $Y[n]$ passes the threshold η then a hit is declared and the tracking process is initiated. If the acquisition decision variable $Y[n]$ fails to pass the threshold, then the code phase of the locally generated code is advanced by δ_t and the process is continued. For the analysis we consider the value of δ_t as 1/2, i.e. a step size of half a chip.

III. CORRELATOR CLASSIFICATION

GPS hardware correlators can be classified based on the processing methodology as in Table- 2.

Basis for classification	Type
De-spread Method	Active Parallel Correlator (APC)
	Passive Matched Filter (PMF)
Channel Processing	Sequential
	Parallel
Simultaneous Time Searches	Single Tap
	Multiple Tap
Frequency Search Method	Serial Frequency Search
	Parallel Frequency Search

Table 2 Correlator Types

The following is a brief description of the classification.

A. DESPREAD METHOD

The parallel code search can be either Active Parallel Correlator (APC) or Passive Matched Filter (PMF) type. In the APC approach, at a time, a single received signal sample is correlated with multiple locally generated code taps. Each tap of the code generator is delayed by the code bin step size with respect to the previous tap. In the PMF approach, correlations are performed between a set of consecutive received signal samples (delayed by code bin step size at each tap) and a single local code generator tap.

In other words for PMF, the incoming code phase moves continuously with respect to the fixed local code segment, while the phase of the local code segment moves with respect to the incoming code in APC [11]. The performance of both APC and PMF methods are analyzed in [9]. It is shown that for a fixed receiver computational rate and moderate to large frequency uncertainties, the performance of the APC search implementation is generally superior to that of the PMF approach. Since the Active Parallel Correlator and the Passive Matched Filter are mathematically equivalent, the proposed method considers only the APC search scheme.

B. CHANNEL PROCESSING

In a correlator, the channel processing can be parallel or sequential. In the parallel scheme, correlation for all channels is accomplished by having dedicated hardware resource for each channel. The minimum required operating frequency of the correlator circuit is same as the sampling frequency. In the sequential scheme, a single correlator resource is time multiplexed among all channels [10, 15]. Here the minimum required operating frequency of the correlator circuit is $C \cdot f_s$ where C is the number of channels and f_s is the sampling frequency. The proposed method employs sequential scheme.

C. SIMULTANEOUS TIME SEARCHES

Single tap refers to a correlator that performs correlation between a single received signal sample and a single local replica code. In Multi tap and All-tap schemes more than one correlation value is obtained simultaneously. Multi tap schemes can follow either APC or PMF searches. All-tap refers to the case where the number of simultaneous code searches is equal to the code length L. The proposed scheme employs a Multi tap APC search scheme.

D. FREQUENCY SEARCH METHOD

The frequency uncertainty region can be searched in frequency steps (equal to the required frequency bin size) as in Serial frequency search schemes. As explained in earlier, in Parallel frequency search schemes multiple frequency bins are searched simultaneously using Discrete Frequency Transform. In the parallel search scheme, the number of simultaneous frequency bins is determined by the Integrate and Dump filter. For large frequency uncertainties, the total number of frequency bins is partitioned using smaller number of frequency bins (segments) [12]. The proposed scheme considers segmented parallel frequency search method.

IV. SEQUENTIAL MULTI-TAP CORRELATOR

Previous sections listed few possible architectural variants of the correlator. We propose a new correlator based on Sequential-Multi-Tap APC approach.

Typical sample rate in a conventional correlator (δ_t =1/2) is much less than the maximum possible operating frequency of a correlator channel circuit. This makes it possible to time-multiplex hardware resource of a single correlator among all channels. The overhead incurred for this operation is the storage requirement for Digitized IF samples. This is the normal time-space trade-off issue and can be resolved considering the system architecture and the application.

Using Multi-tap correlator within the conventional correlator framework reduces the search time by a factor R. Here R represents the number of code taps that are searched "simultaneously". If we incorporate the multiple code taps in parallel channel scheme, then hardware requirements will increase significantly. This is not the case in sequential channel scheme, as there is only one channel. Hence the trade off (improved MAT for a small increase in hardware resource) is very justifiable in this case.

A. SYSTEM DESCRIPTION AND DECISION LOGIC

A part of the correlator is shown in Figure-3. The inputs to the decision logic module are the envelope of correlation values of all taps. The decision variable is a function of $Y[n], Y[n+1], \ldots Y[n+R]$.
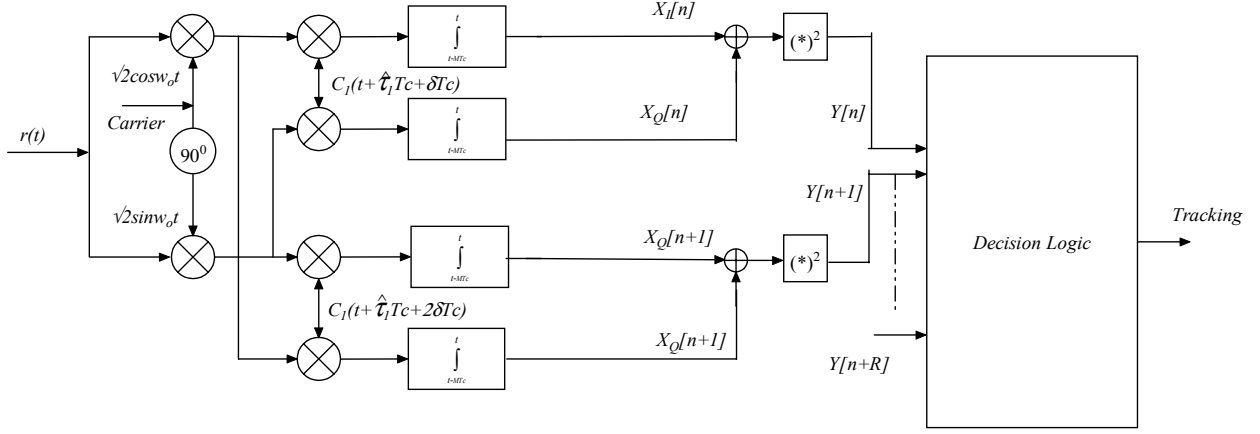
Figure 3: SMT Correlator Structure

The search procedure with the new decision variable is as follows. Let η be the threshold set for making a decision when the received PN sequence and local de-spreading PN sequence are within a desired timing offset (in our case (δ_t=1/2), so as to terminate the acquisition procedure and switch to tracking mode. The decision variable is computed as $\max(Y[n], Y[n+1], \ldots Y[n+R])$.

Whenever the decision variable exceeds the threshold η, the decision logic selects corresponding *X[n]* and the corresponding delay as the estimated delay. Effectively we search R time cells in parallel. At each step if the decision variable does not exceed the threshold _ the relative phase of the local PN sequence is updated to the next test code delay (advanced by R chip shifts) and the testing process is repeated. The search pattern can be selected appropriately (for example zigzag search), so as to minimize the effect of code doppler on the mean acquisition time [11].

V. REALIZING SMT CORRELATOR

A. BASIC BUILDING BLOCKS

The GPS correlator processes the digitized IF data received from a GPS RF front end. The basic building blocks of a GPS correlator are

1. *Local Carrier Generator*

Local carrier is generated using a Numerically Controlled Oscillator (NCO). The Sine and Cosine components are generated with SIN/COS Look Up Table (LUT) [2]. The width of the accumulator in NCO is selected based on the

sampling frequency and required resolution. The number of bits required for phase quantization and amplitude

quantization are selected based on required Spurious Free Dynamic Range (SFDR) and quantization loss respectively. The local carrier frequency generated will be $f_l = f_s - f_{IF}$ during satellite acquisition process.

2. *Quadrature (complex) Carrier Mixer*

The inputs to the mixer take any one of the fixed values (due to quantization) and the mixer is realized as LUT. In-phase and quadrature-phase outputs are provided to the succeeding stages.

3. *Replica Code Generator*

The replica code generator consists of following sub blocks.

i. *Code NCO*

The input clock to code NCO is the sampling clock frequency. The NCO generates a frequency, which is the sum of chipping frequency of 1.023MHz and any code doppler frequency. The MSB of the NCO register gives the clock for C/A code generator). The clock for the shift register (half chip spacing clock) is derived from second MSB.

ii. *C/A code generator*

GPS C/A code is a 1023 length Gold code [3]. The C/A code generator is realized with two 10 bit shift registers and a phase selector for selecting different PRN numbers. The chipping clock generated by the code NCO clocks these shift registers.

iii. *2R-bit Shift Register*

The code bit from the C/A code generator is clocked into the 2R shift register at half chip spacing clock derived

from NCO. This shift register determines the number of simultaneous time cell searches.

4.   *Code Mixer*

The code mixer multiplies the received signal sample with the local code. Multiplication of the received signal with the reference PN code is achieved by performing an XOR operation. If the reference PN code is zero, the input sample to the code mixer is negated. For the coupled and decoupled addition schemes, two local code taps delayed by half chip are added before performing XOR operation. Note that we need 2R code mixers for correlating all the bits of the shift register with each arm of the carrier. The code mixer output is input to the Accumulator.

5.   *Accumulator (Integration and Dump)*

Before initiating the correlation process, the accumulators are cleared. Code mixer output is accumulated for both in-phase and quadrature arms separately. After a predetermined duration of accumulation, the accumulated values are saved and accumulators are cleared before starting next accumulation. The duration of integration time determines the allowable doppler frequency uncertainty window Δ_f.

B. ARCHITECTURE OF SMT CORRELATOR

The block diagram of SMT correlator with R = 10 is shown in Figure 4. The interconnection of basic blocks is depicted in the Figure.
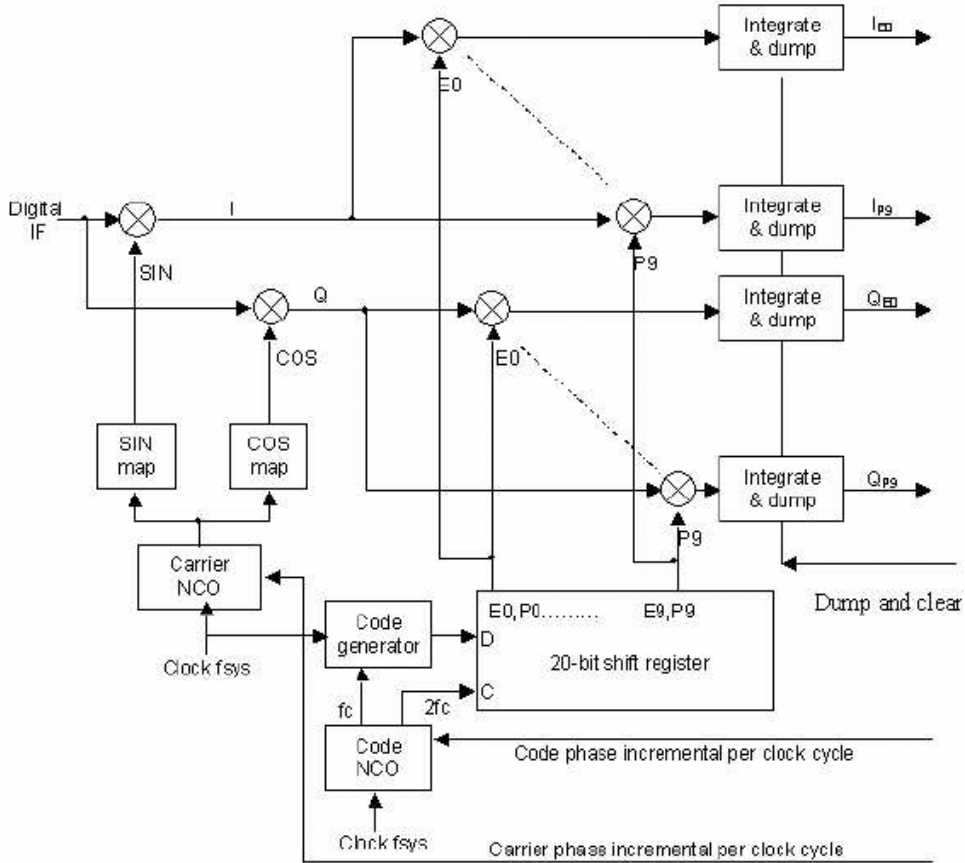

Figure 4: A 10-tap sequential correlator

Since this is a sequential channel-processing scheme, the Carrier NCO and Code NCO are clocked by system clock (which is slightly greater than $C \cdot f_s$). δ_t =1/2 results in

20 code mixers for both inphase and quadrature arms. E0... E9 are the half chip early samples of the local code

and P0… P9 are prompt samples of the local code. After the ID process 40 correlation results (IE0; IP0…IE9; IP9 and QE0; QP0…QE9; QP9) are obtained. It can be shown

that non-overlapping addition of half chip separated correlation values results in negligible degradation in probability of detection. This leads to 20 effective accumulators for the SMT correlator with R=10.

C. ADVANTAGES OF THE SMT CORRELATOR

Apart from the reduced acquisition time, the SMT correlator has significant advantages in gate complexity for the same performance index. This section gives the equivalent gate complexity details for the proposed correlator scheme in comparison with the conventional correlator scheme. Equivalent gate complexity is computed using gate counts of basic units, which are common to both correlators, as well as overheads in both architectures.

The sequential multi-tap correlator has to store some critical channel parameters (like carrier NCO register value, code NCO register value etc.) to enable multiplexing of channels. This involves a control block to generate timing signals and a storage block to hold the channel parameters through one channel cycle. This overhead compared to the conventional correlator is referred here as "channel switching" activity. A 12-channel (10-tap in case of SMT) correlator is chosen for the comparison.

	Number of blocks required	
	Conventional	SMT
Local Carrier Generator	12	1
Complex Carrier Mixer	12	1
Replica Code Generator	12	1
Code Mixer (I and Q)	6 (3 code arms)	40
Accumulators	36	40
Channel Switching (Control and Storage)	NA	1

Table 3: Requirement of basic building blocks

As we can see from the table above, the hardware required by the carrier generator, carrier mixer and code generator are reduced by a factor of number of channels (12 in our case). Increase in the number of accumulators in the SMT correlator is insignificant, since the conventional correlator has 3 code arms, but they are 'contained' in the multi-tap architecture itself. Number of code mixers increase significantly by 6 to 40 but this does not increase the gate count since each code mixer performs simple (3-bit negation) operation. Channel-switching activity requires additional hardware, which involves control logic and memory space. In reality, this additional hardware requirement is much less than the advantage gained in other correlator blocks.

VI. TEST RESULTS

A. MEAN ACQUISITION TIME

Figure-5 shows normalized acquisition time, that is MAT/Tc for conventional scheme and the SMT correlator scheme. For comparison, a 20-tap correlator was used. The correlator parameters that were used for the comparison are

1. GPS C/A code (length = 1023, $T_c = 1\text{ms}$)
2. Integrate and Dump duration $M = 64$
3. Number of satellites in view $K = 12$
4. False alarm penalty $J = 2^6 = 64$

5. Normalized threshold $= \dfrac{2\eta}{N_0 M T_c}$

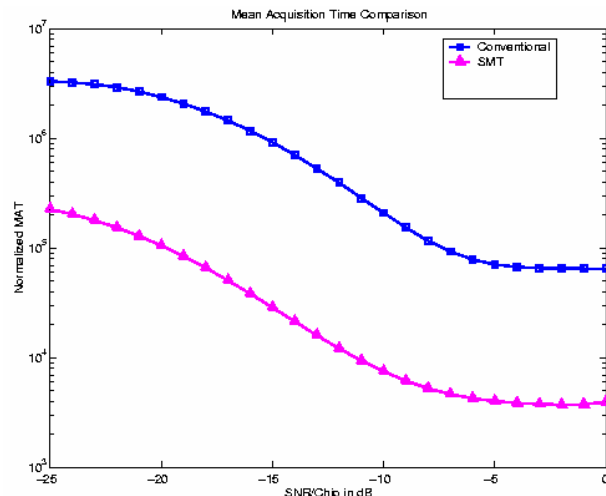6. SNR per chip $\gamma = \dfrac{E_c}{N_0} = \dfrac{S T_c}{N_0}$

Figure 5: Mean Acquisition Time Comparisons

B. TTFF

The proposed scheme improves TTFF by improving the Mean Acquisition Time. Table- 4 shows the improvement in TTFF of the GPS receiver, which employs SMT correlator over the receiver that uses conventional

scheme. Both bench tests and field tests were conducted and the results show the averages taken over several trials. For comparison, a 12-channel GPS receiver is used. In addition, signal strength of –136dBm is assumed for the comparison.

	Conventional	SMT
Cold Start	70	41
Warm Start	45	30
Hot Start	8	3

Table 4 Typical TTFF Comparisons

C. GATE COMPLEXITY

Equivalent gate (two input NAND) complexities for both the conventional and SMT correlator is shown in Table-6. The gate complexities in the table are including input signal management and the host communication modules apart from the correlator. The host communication module involves transferring correlation and measurement values to a host processor, as well as programmability of several correlator parameters.

12 channel conventional correlator	160K
12 channel 10-tap SMT correlator	75K

Table 5: Gate Complexity Comparison

VII. CONCLUSION

A 10-tap sequential correlator improves MAT by an order of magnitude compared to the conventional correlator. In addition, the sequential correlator is implemented with minimal hardware overhead. The low gate count advantage makes it a potential candidate for integration with other systems.

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